



**FIG. 1**  
**PRIOR ART**

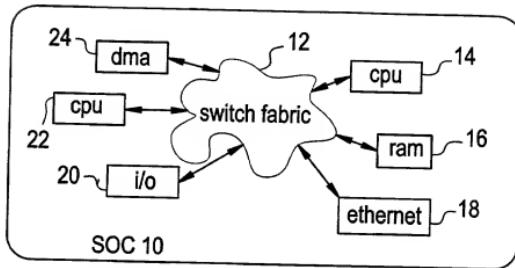


FIG. 2

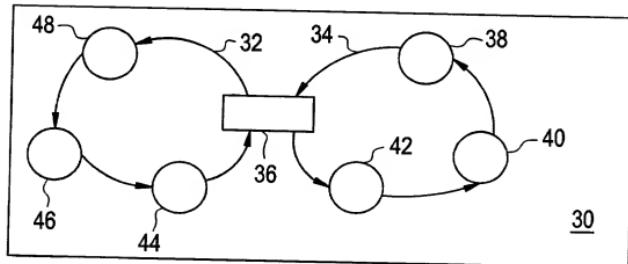


FIG. 3

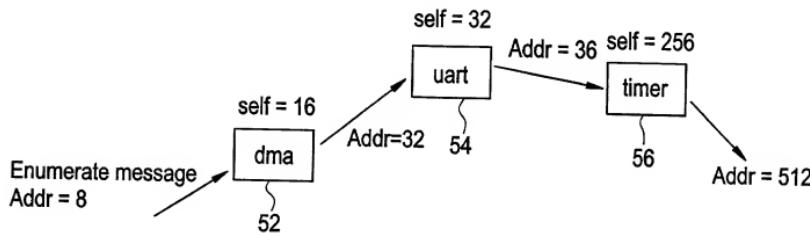


FIG. 4

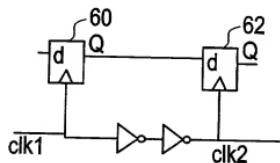


FIG. 5

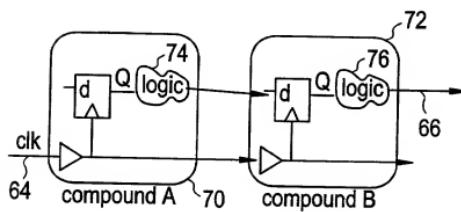


FIG. 6

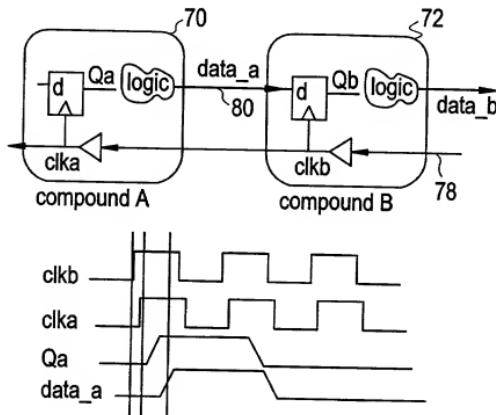


FIG. 7

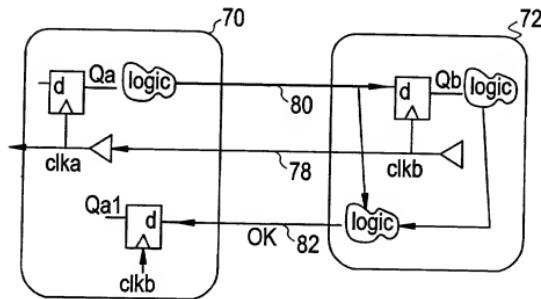




FIG. 8

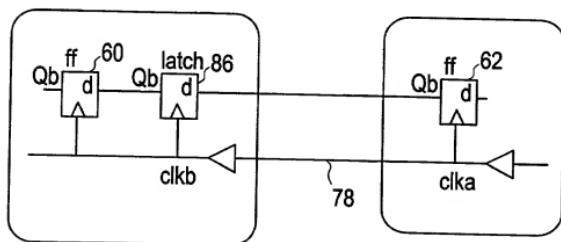


FIG. 9

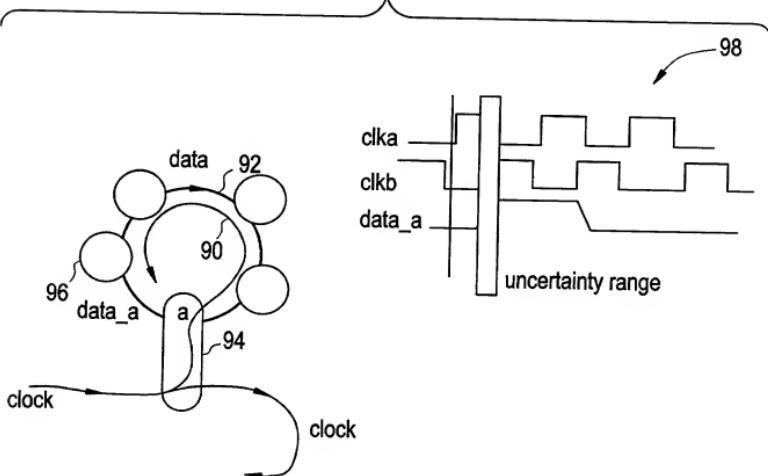
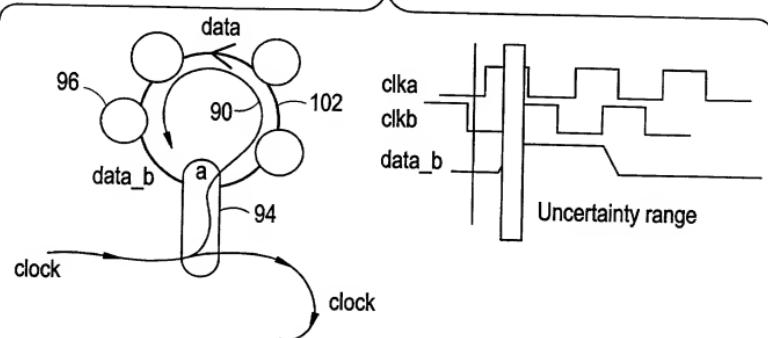


FIG. 10



10244337, 000440

FIG. 11

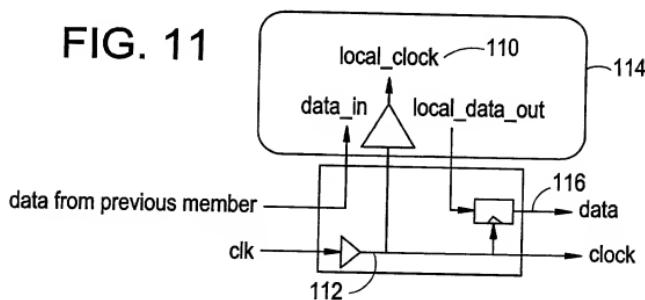


FIG. 12

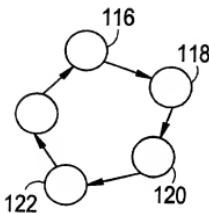
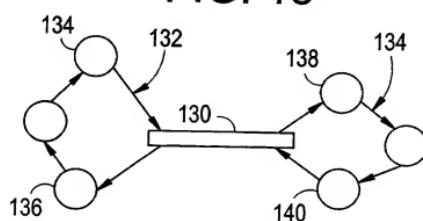
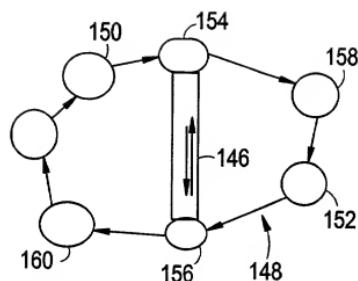
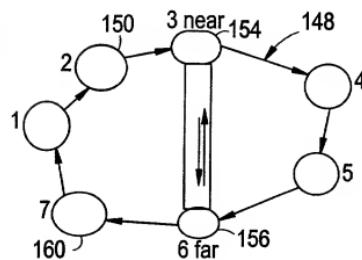
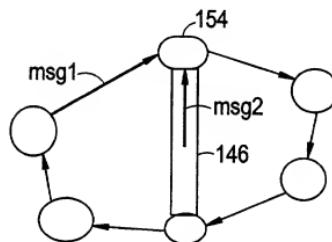


FIG. 13



**FIG. 14****FIG. 15****FIG. 16**

111  
SEP 24 2002  
PATENT & TRADEMARK OFFICE

7/64

FIG. 17

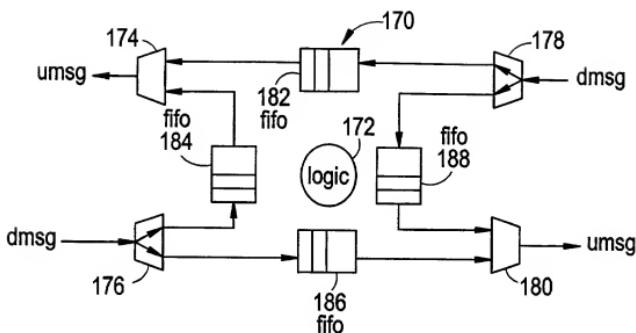


FIG. 18

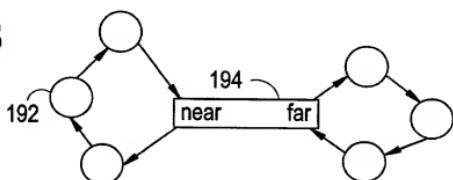


FIG. 19

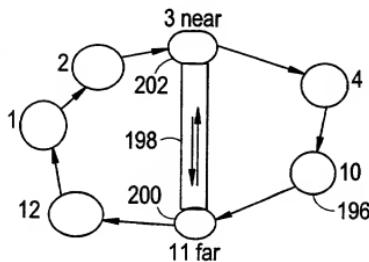


FIG. 20

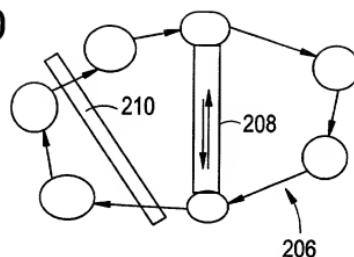


FIG. 21

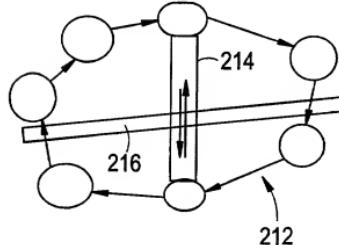


FIG. 22

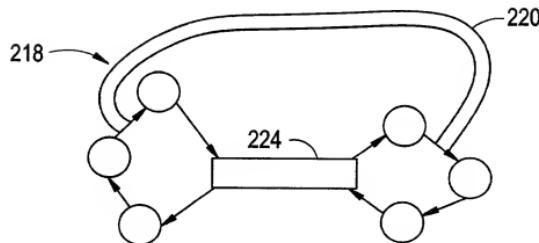


FIG. 23

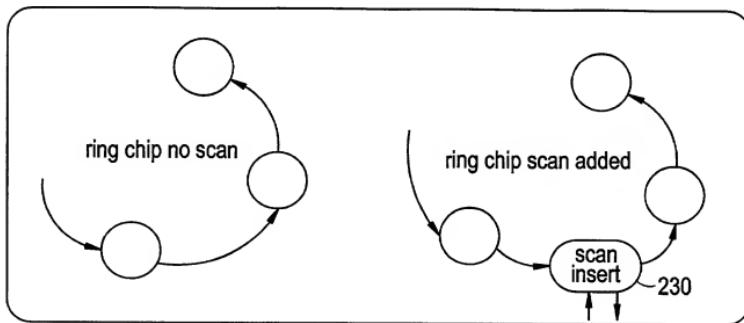


FIG. 24

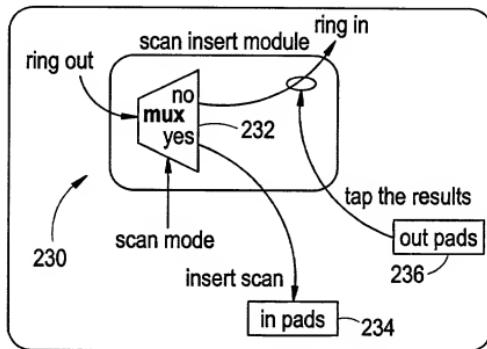


FIG. 25

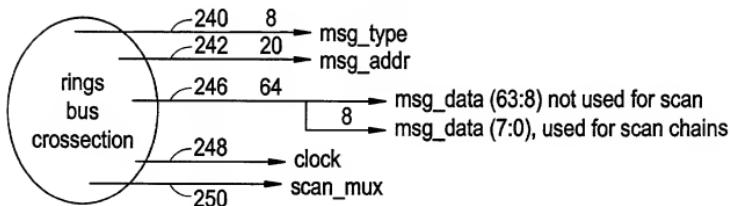
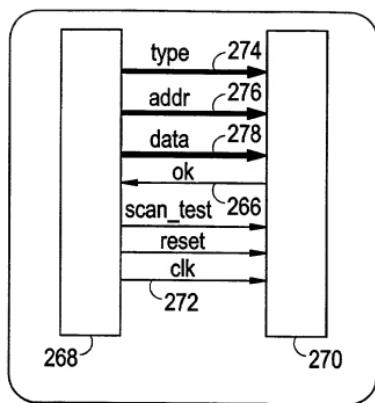


FIG. 26



201260-733907

FIG. 27

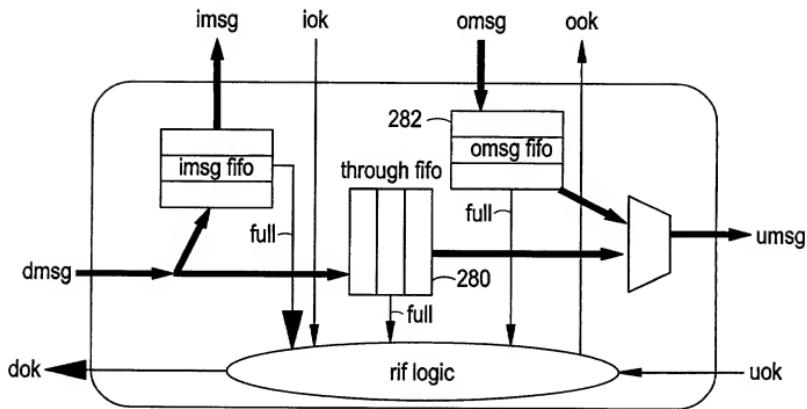


FIG. 28

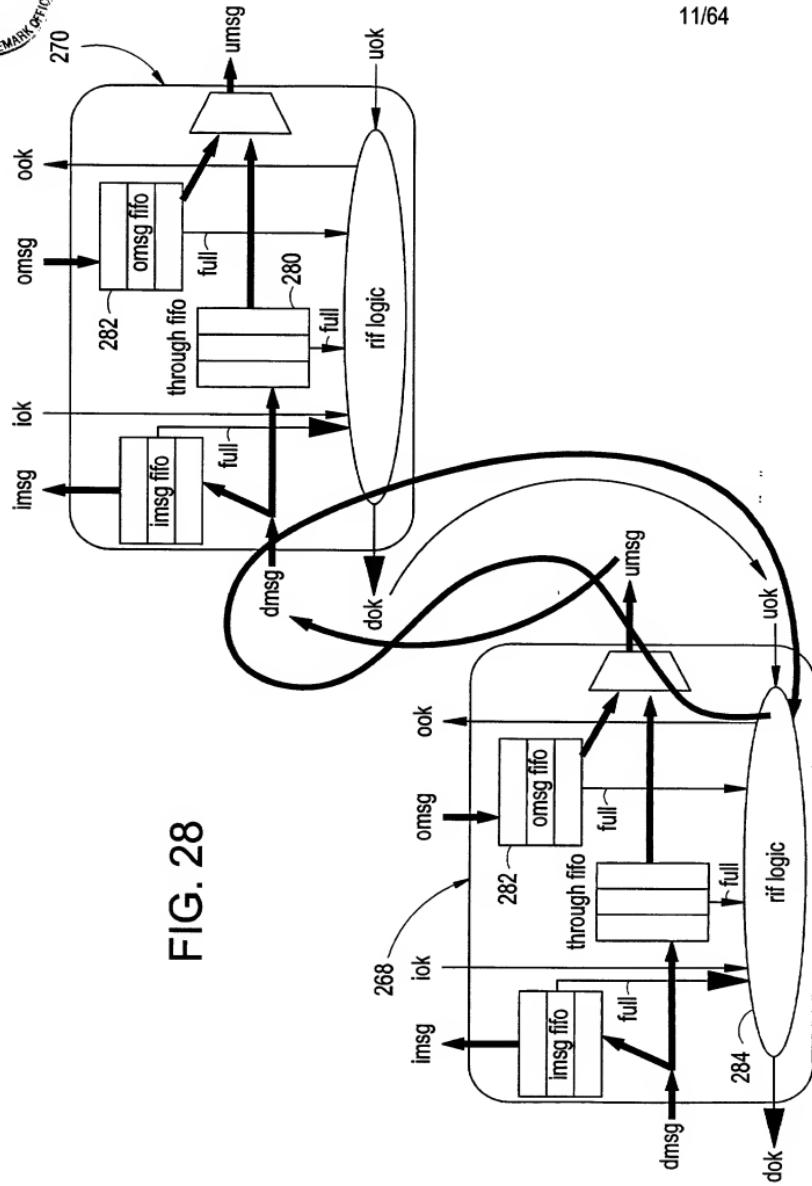


FIG. 29

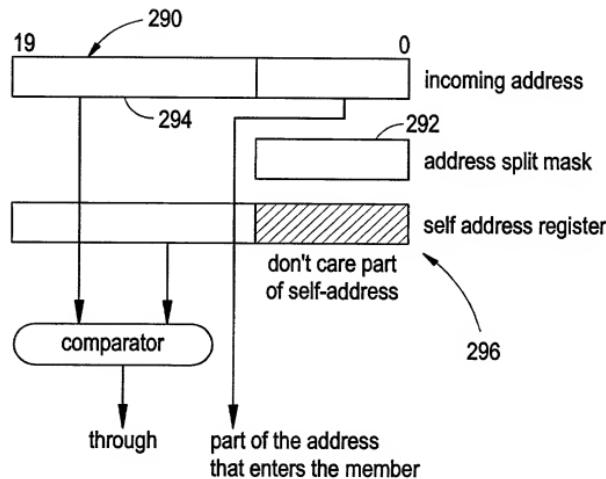


FIG. 30

10064337/092402

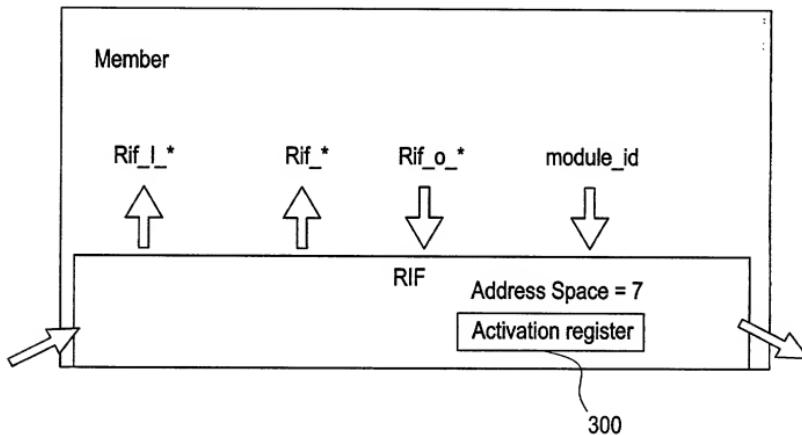


FIG. 31

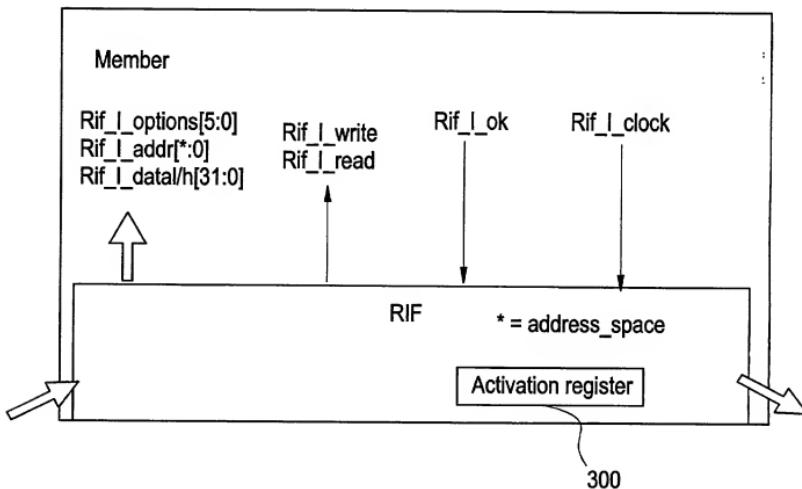


FIG. 32

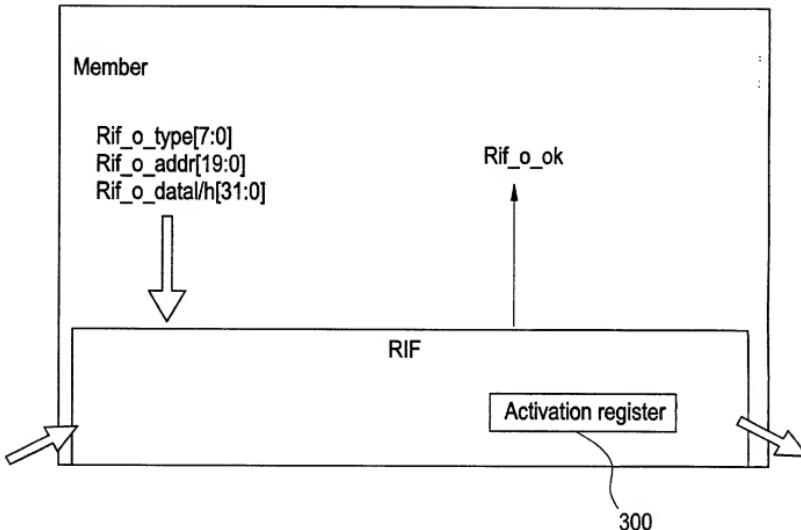


FIG. 33

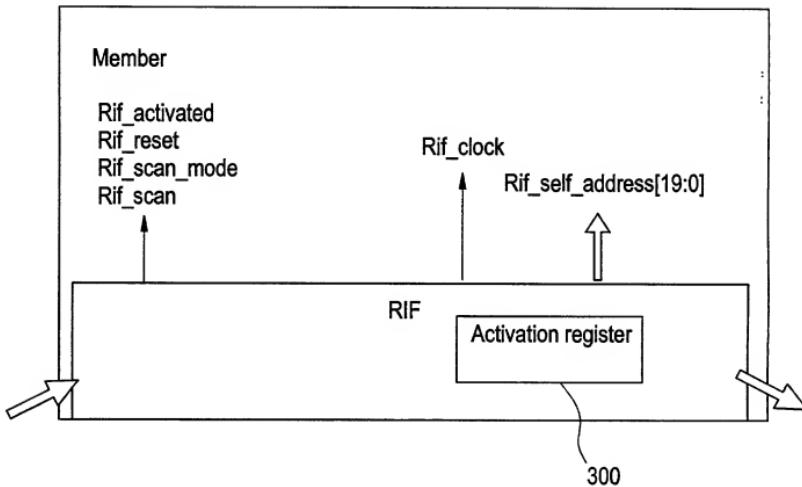


FIG. 34

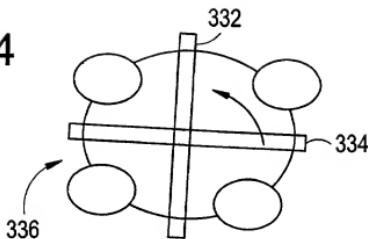


FIG. 35

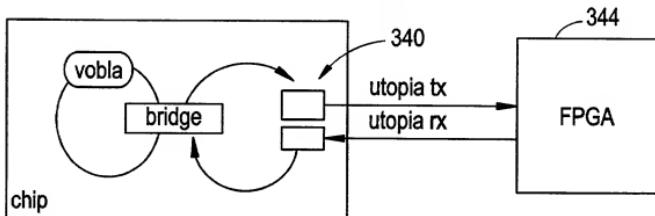


FIG. 36

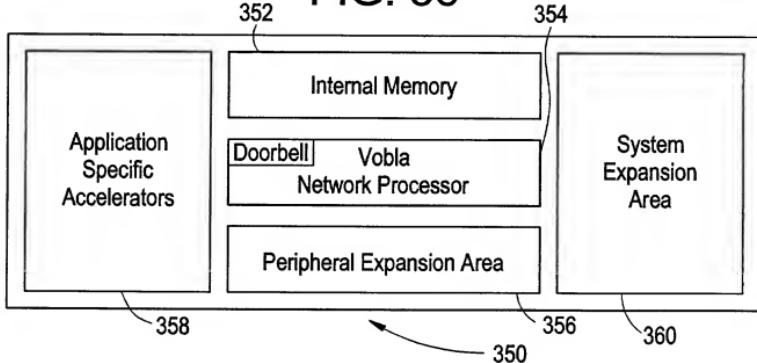




FIG. 37

354  
384

Internal Memory

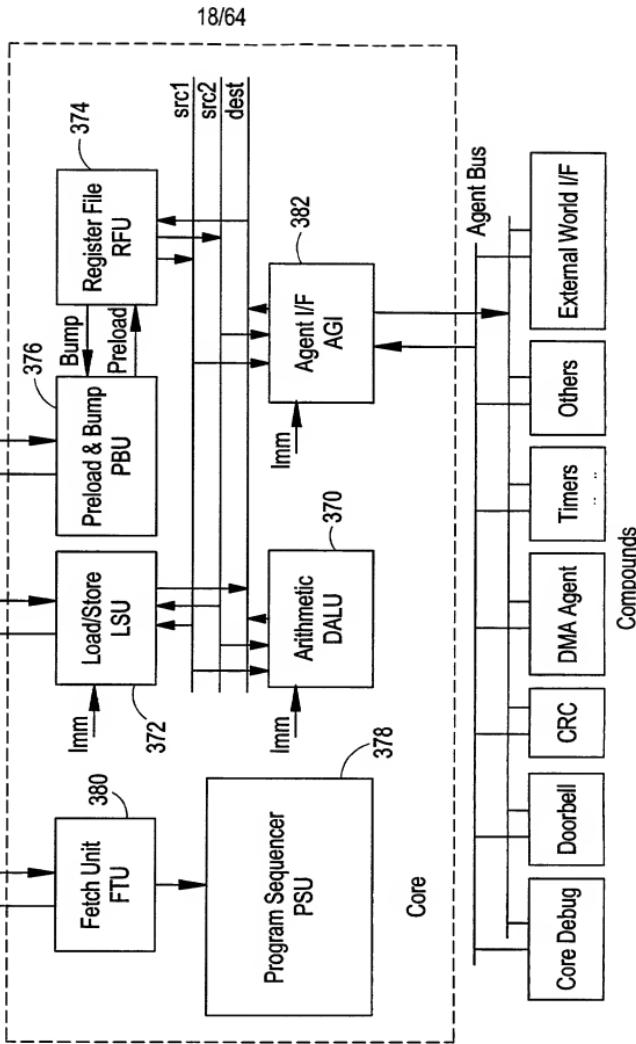


FIG. 38

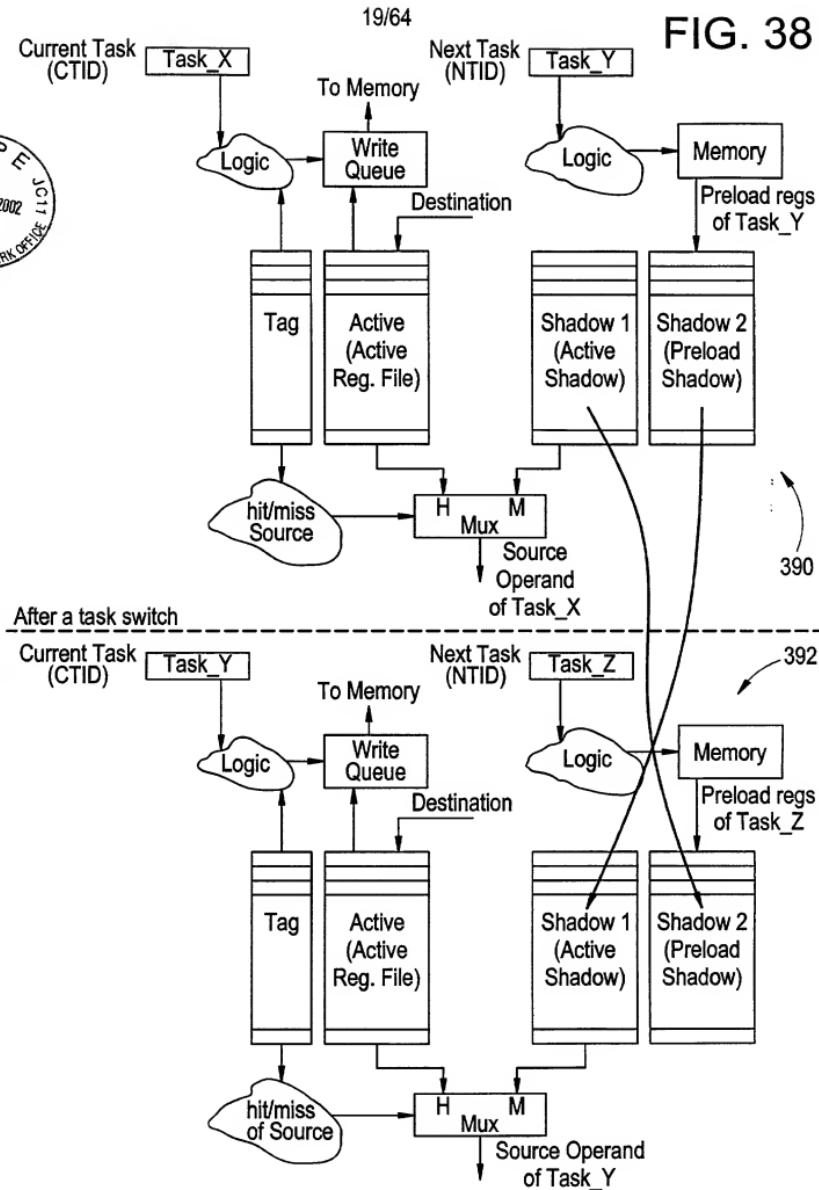


FIG. 39

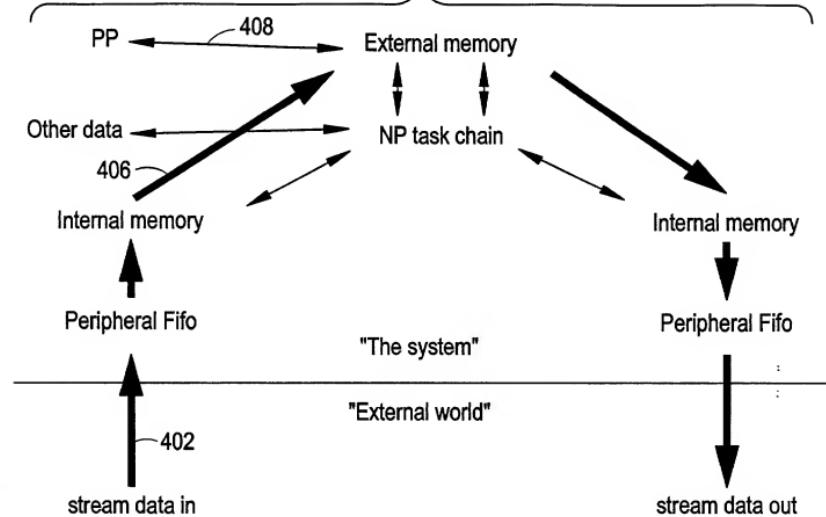


FIG. 40

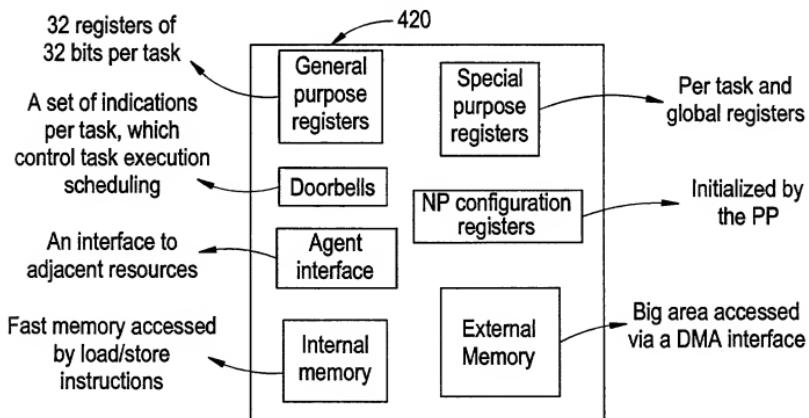
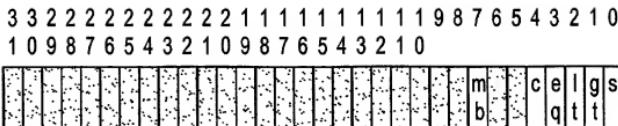




FIG. 41

R1 register



430

FIG. 42

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

REFETCH SPR  
(spr index - 0)

NEXT\_REFETCH

REFETCH

440

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

TASK SPR  
(spr index - 1)

DOOR		COUNT		UMASK		N	NTID		CTID
BELL				R		T			
REQ					V				

442

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

TRAP SPR  
(spr index - 2)

Diagram of the TRAP SPR register showing bit fields and their meanings:

- Bits 31-24: 1111111111111111 (labeled 'Y T D P T D')
- Bits 23-20: 1111111111111111 (labeled 'B B A A R L')
- Bits 19-16: 1111111111111111 (labeled 'B B A A P')
- Bits 15-0: 1111111111111111 (labeled 'P')

444

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

MINDEX SPR  
(spr index - 3)

				INDEX2					INDEX1
--	--	--	--	--------	--	--	--	--	--------

446

FIG. 43

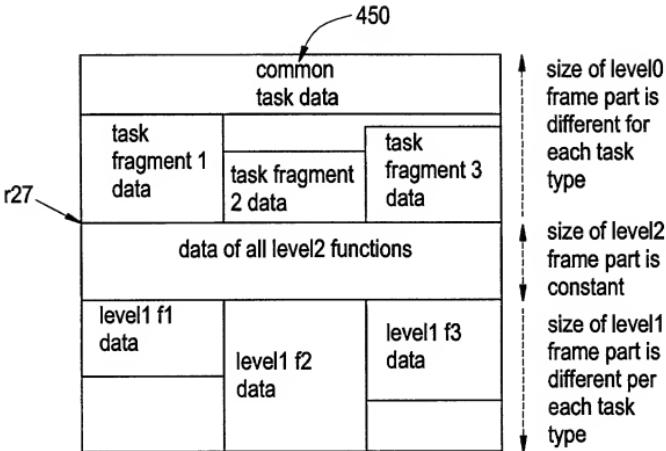
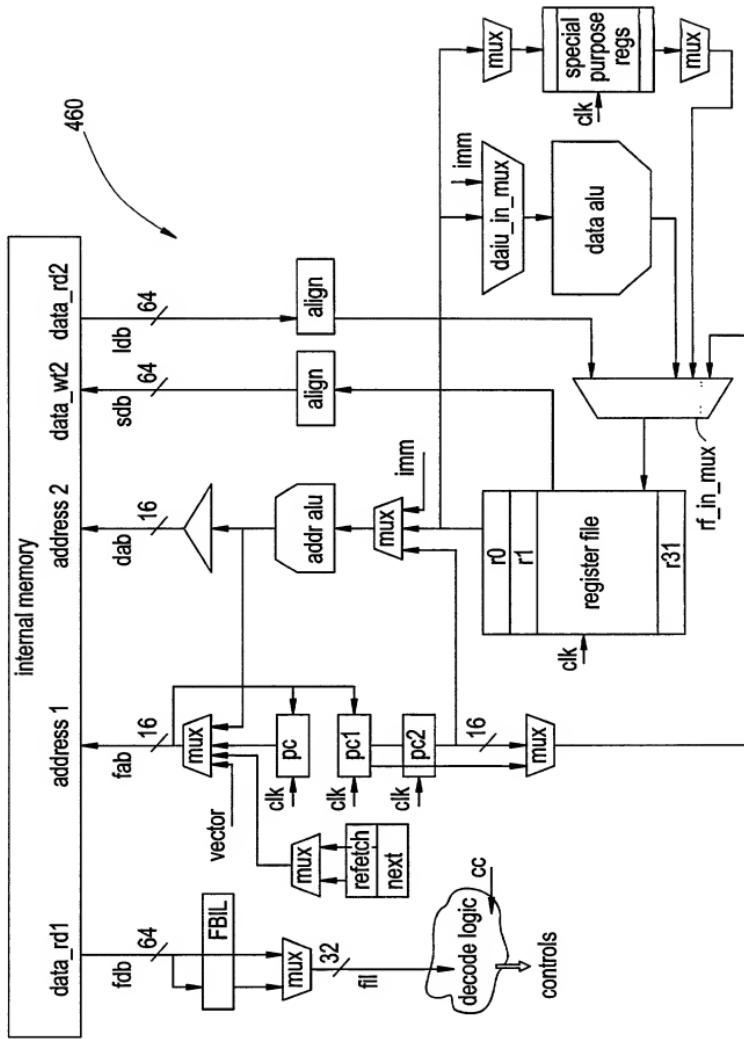
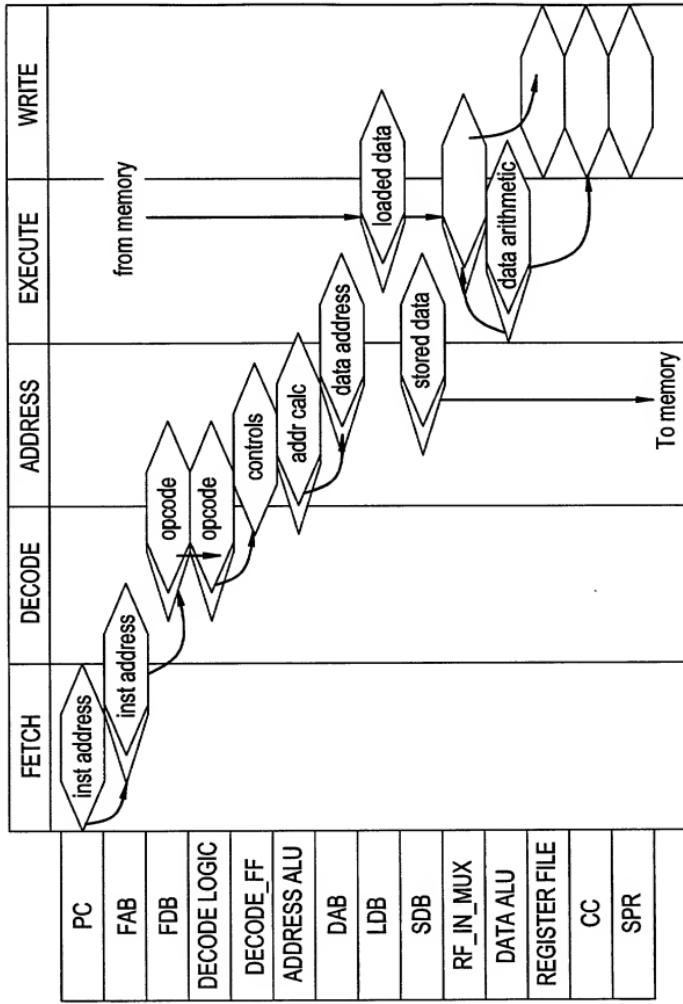


FIG. 44



480

FIG. 45



Logic

## Flip Flop

A small, thin, vertical diamond shape, likely a decorative element or a placeholder for an image.

FIG. 46

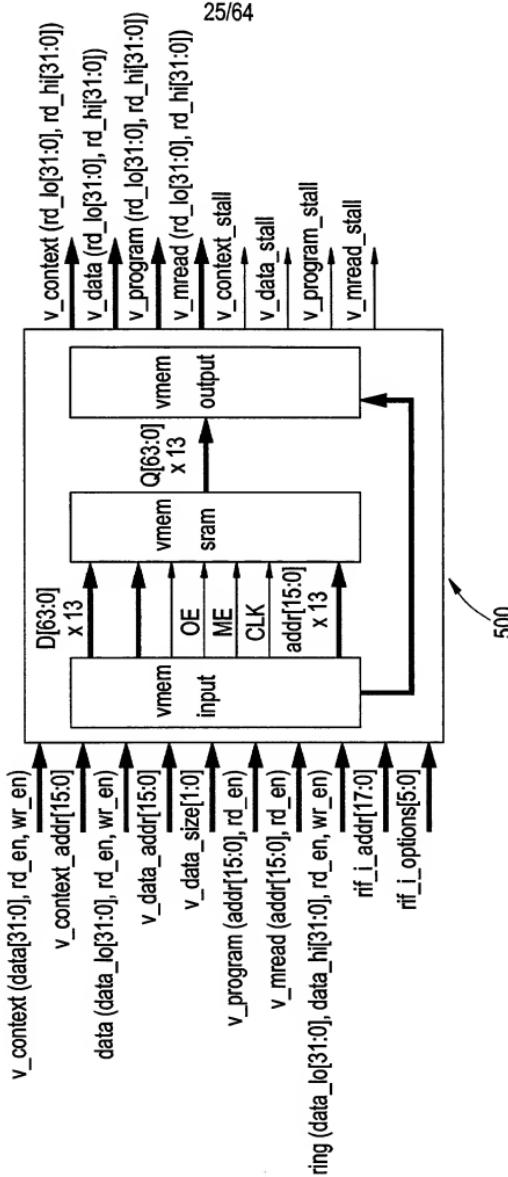


FIG. 47

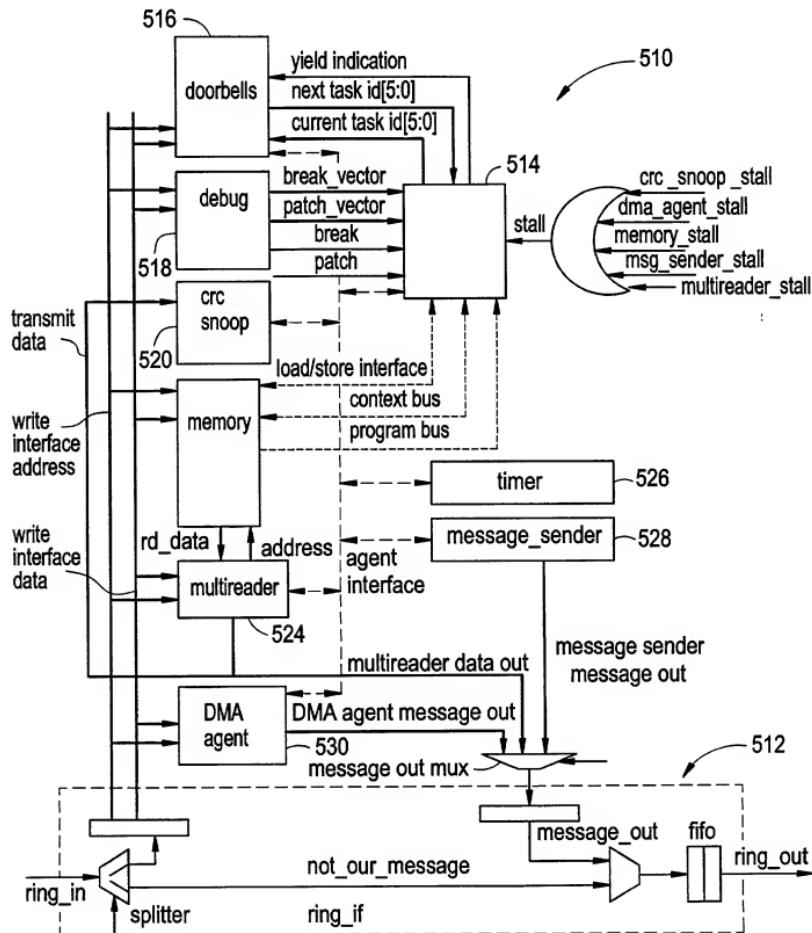


FIG. 48

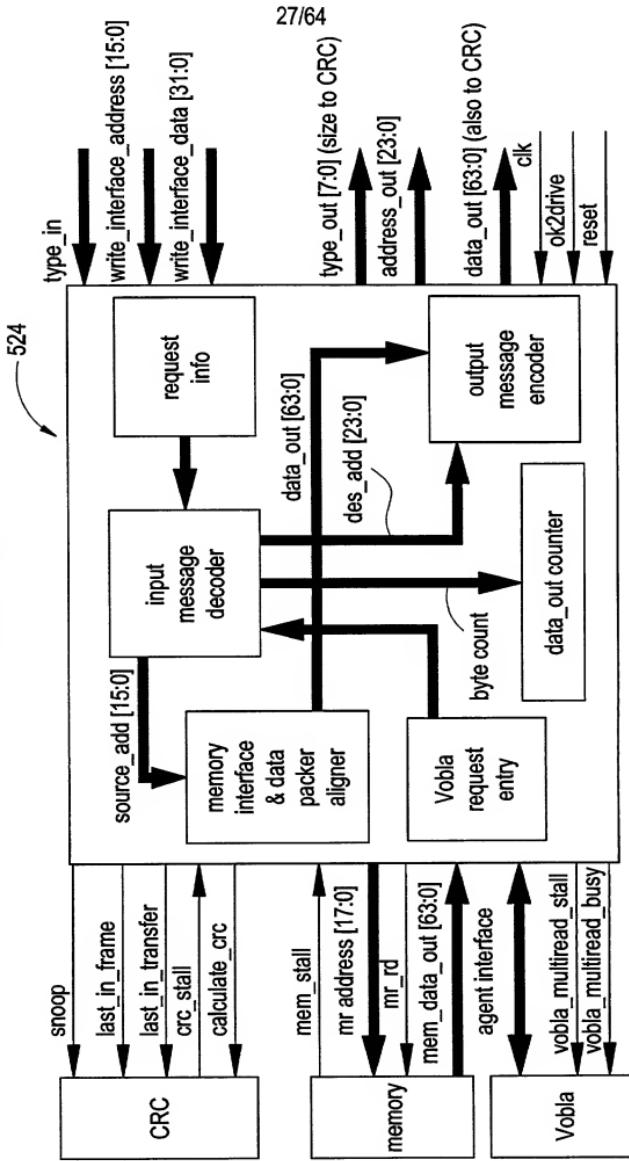


FIG. 49

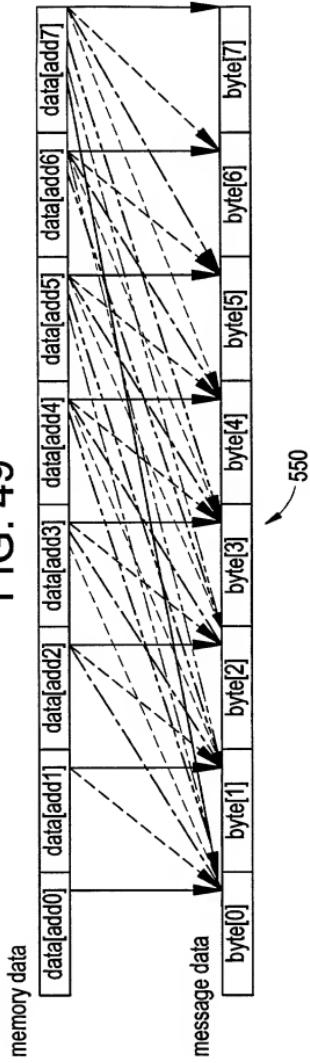


FIG. 50

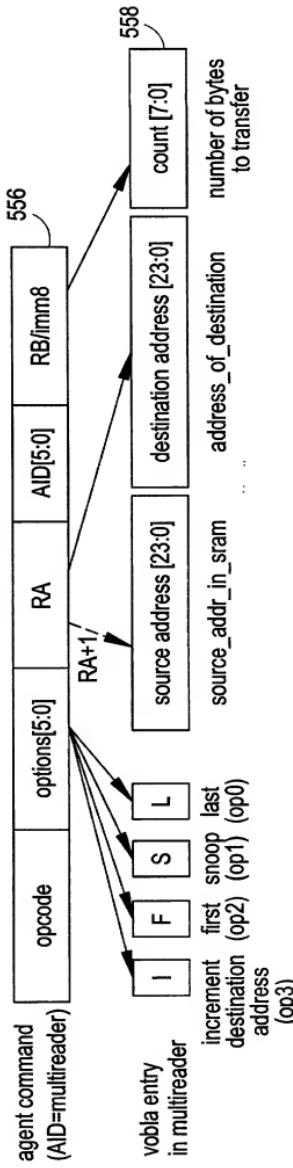


FIG. 51

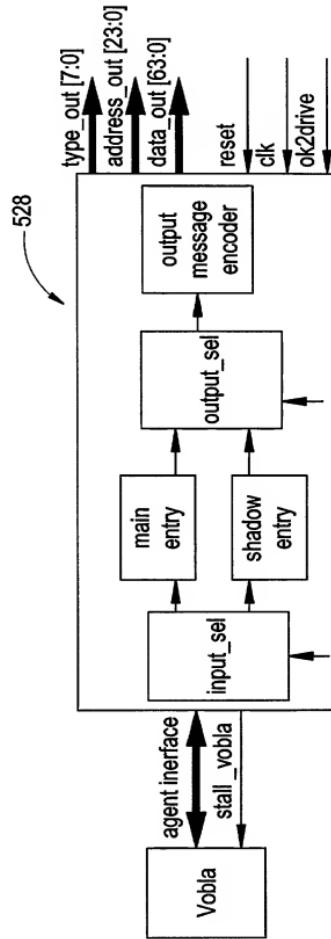




FIG. 52

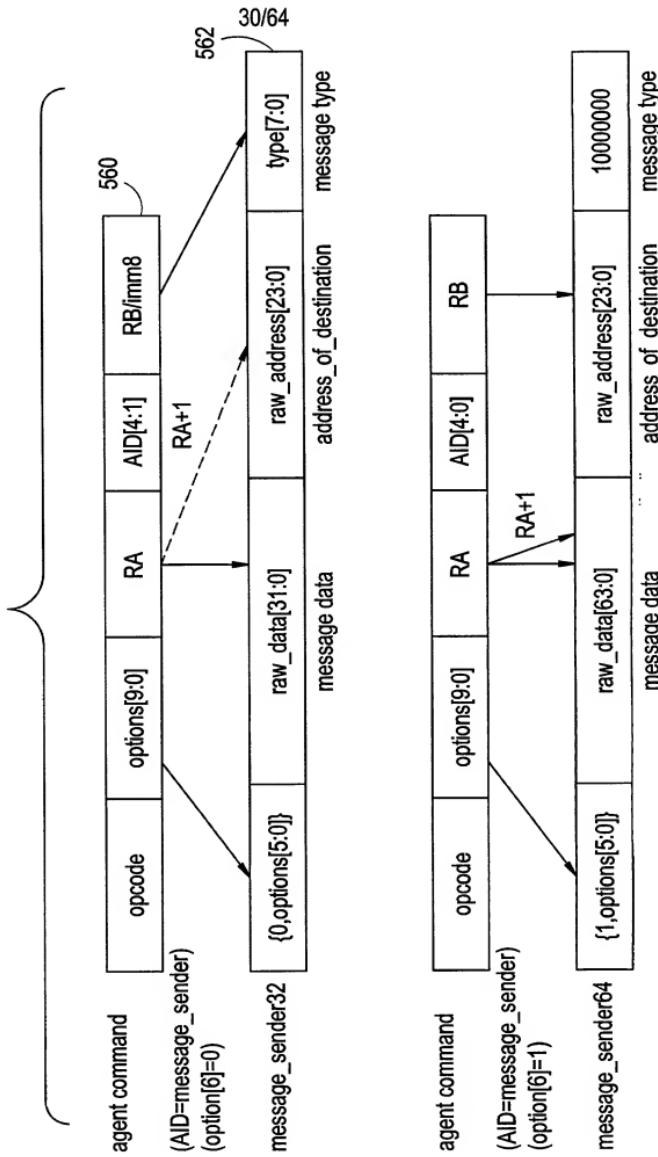


FIG. 53

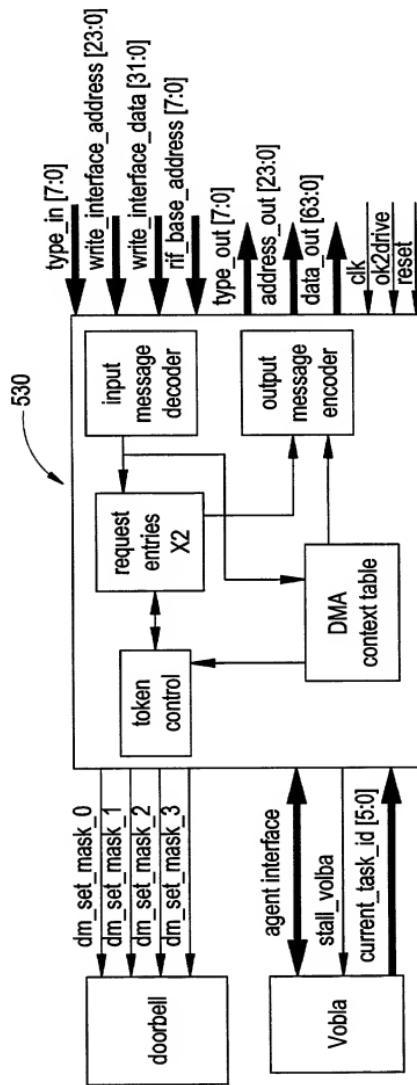




FIG. 54

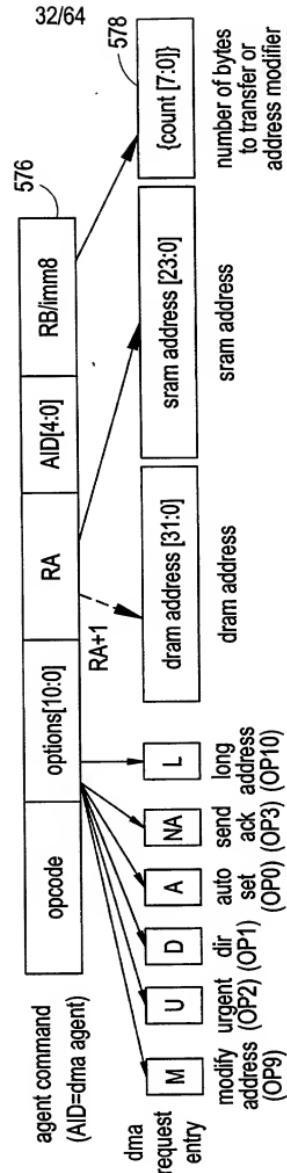


FIG. 55

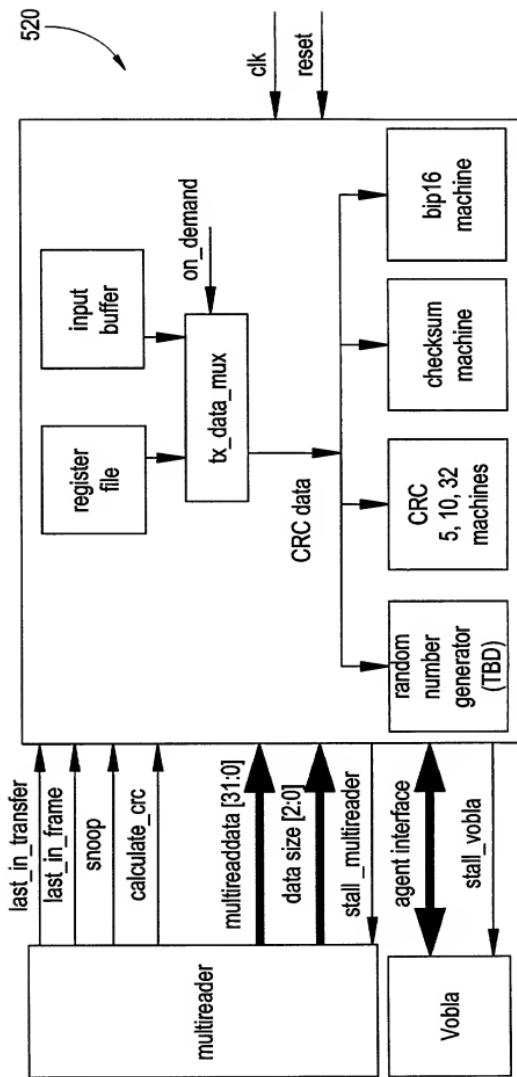


FIG. 56

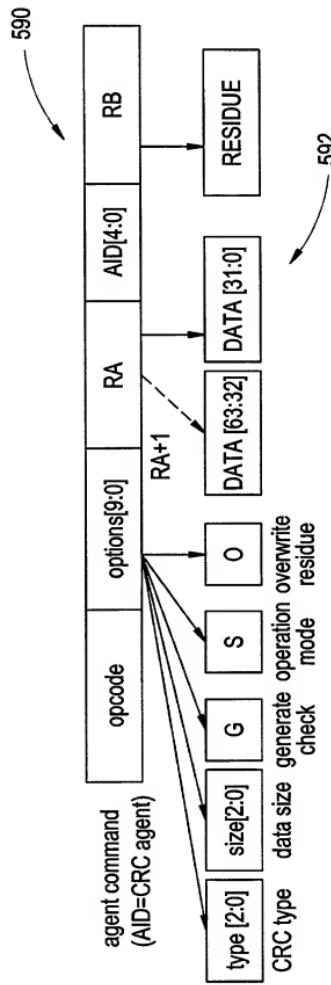


FIG. 57

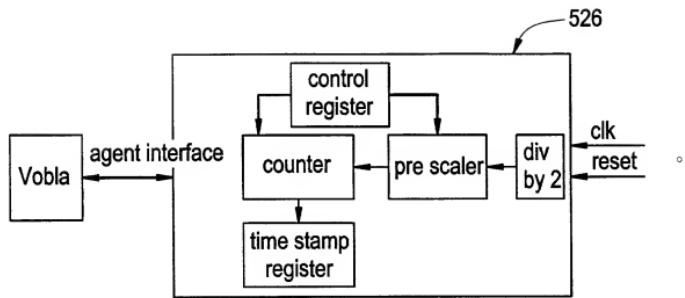


FIG. 58

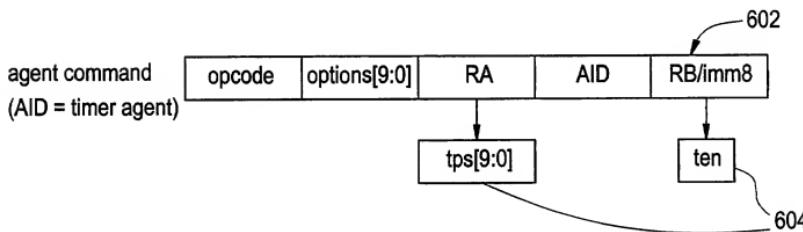


FIG. 59

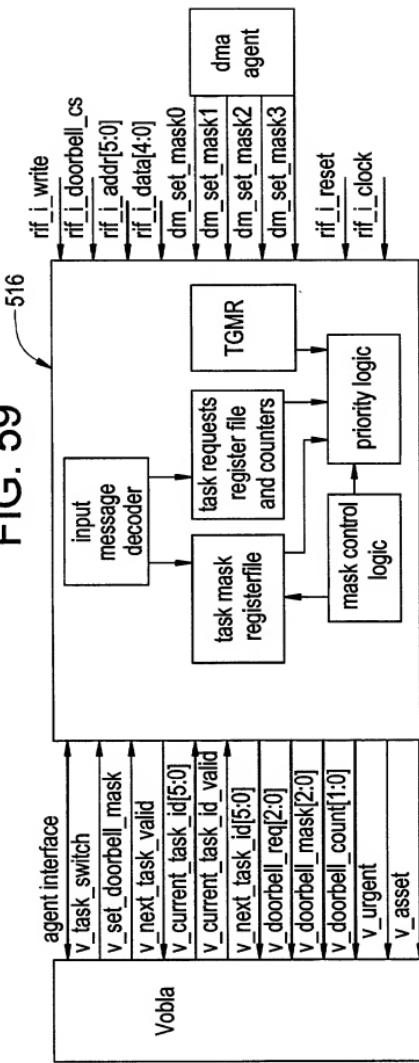


FIG. 60

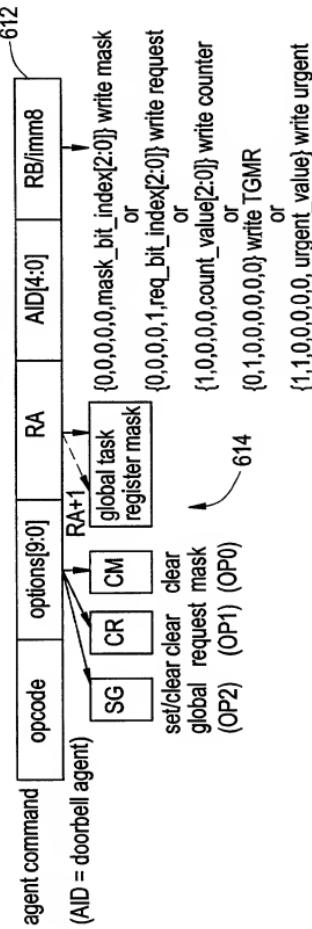


FIG. 61

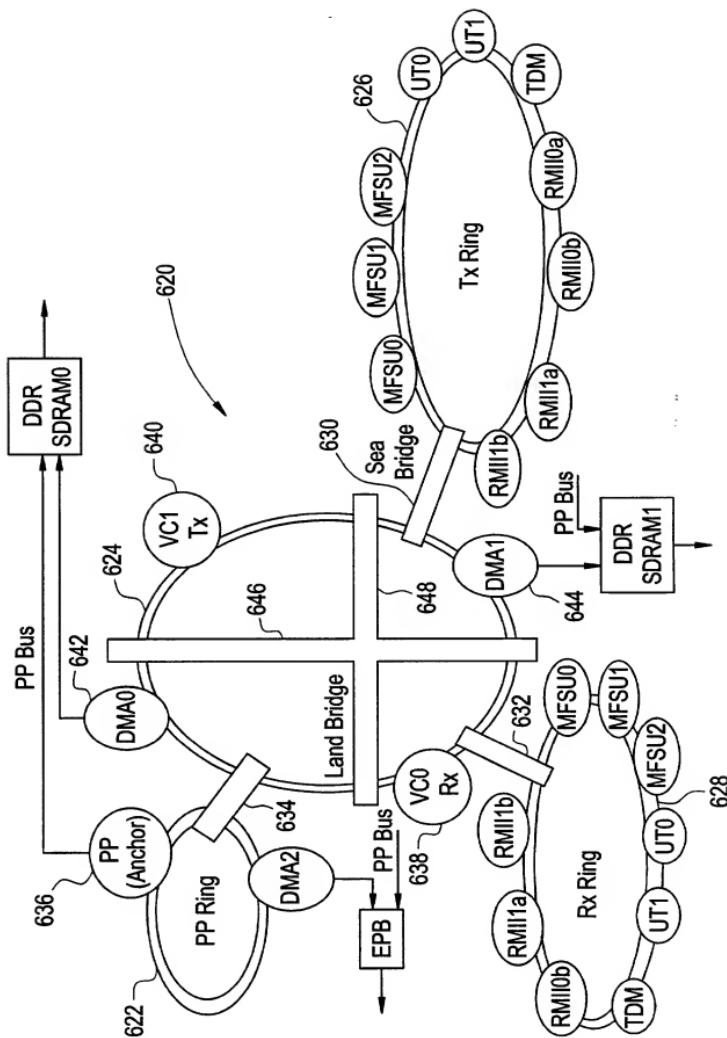


FIG. 62

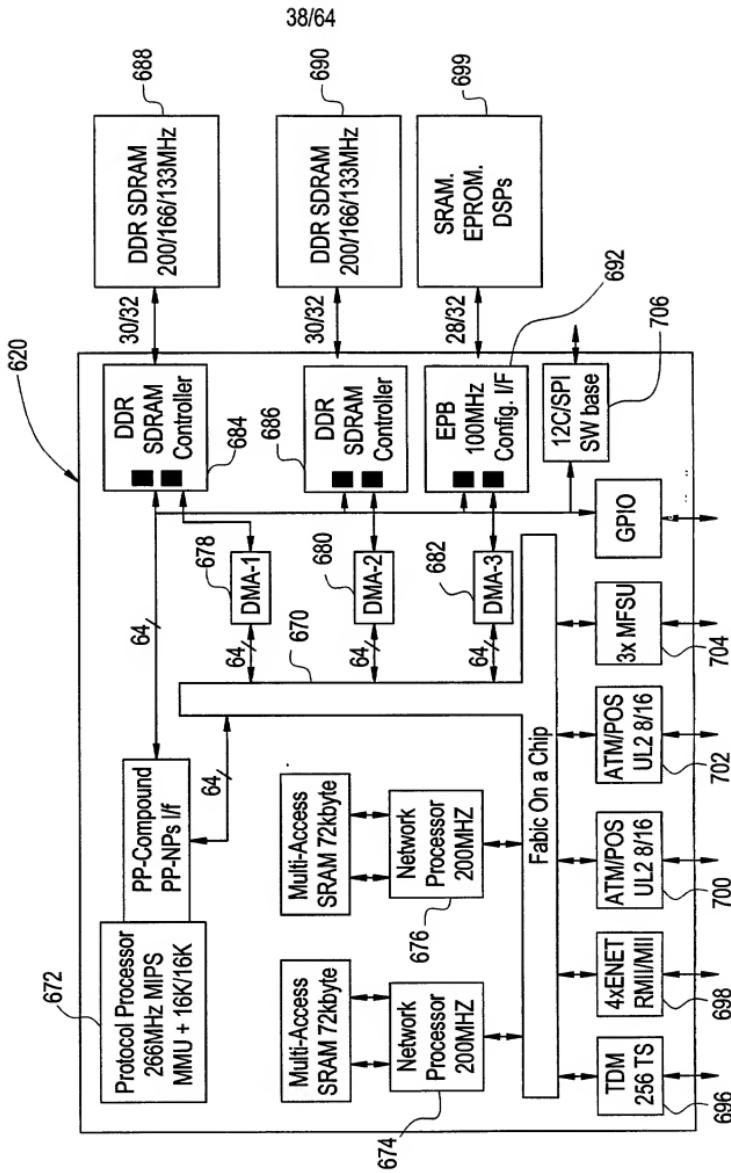


FIG. 63

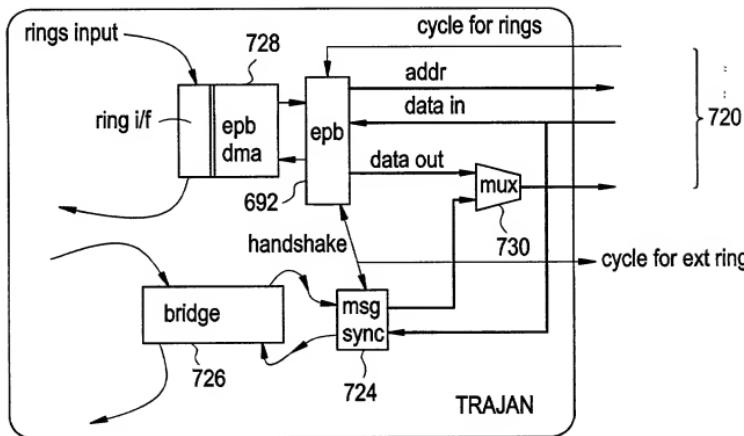
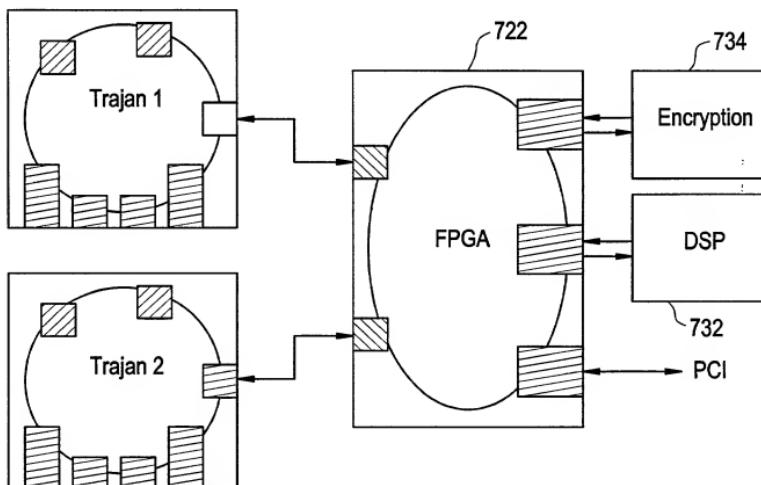


FIG. 64



- Processor
- Functional unit
- External ring interface

FIG. 65

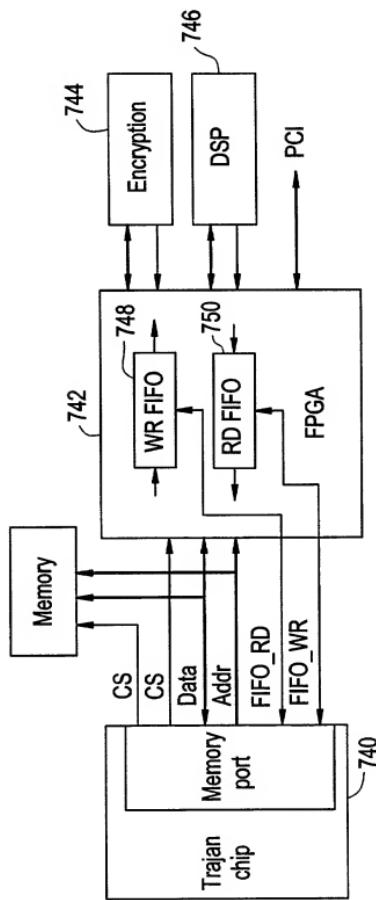


FIG. 66

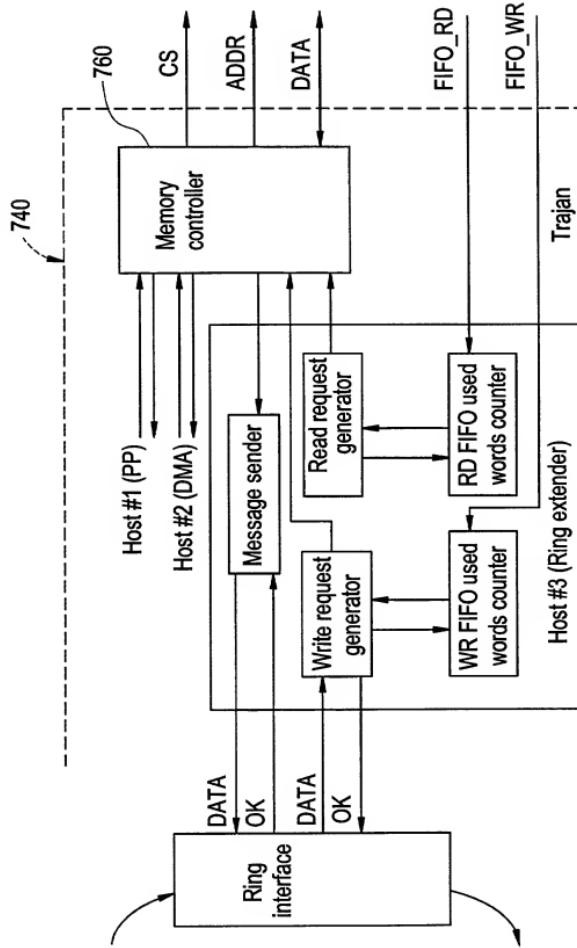


FIG. 67

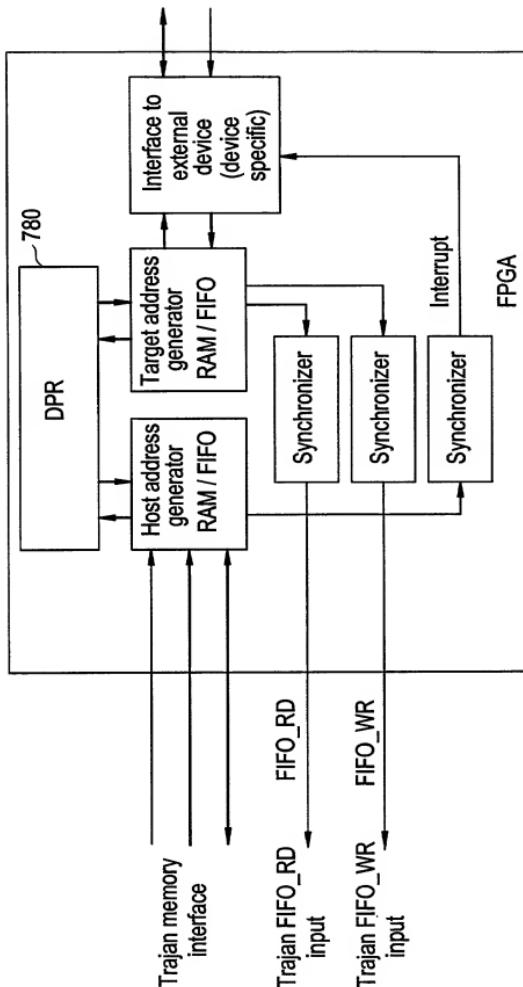


FIG. 68

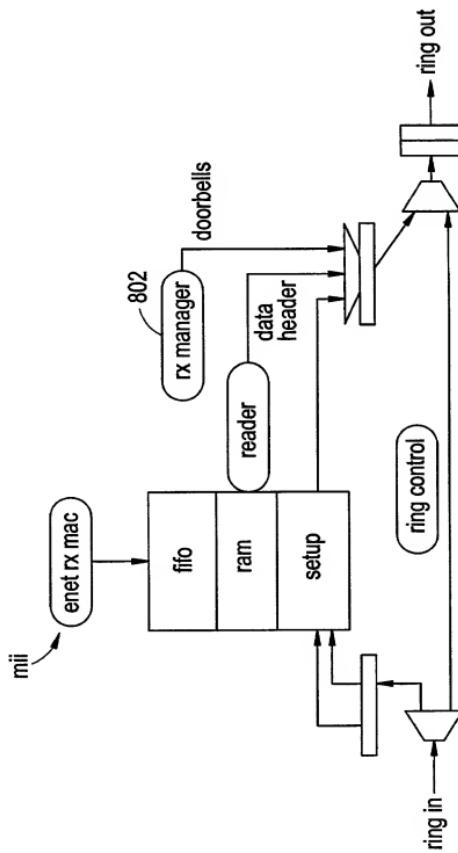


FIG. 69

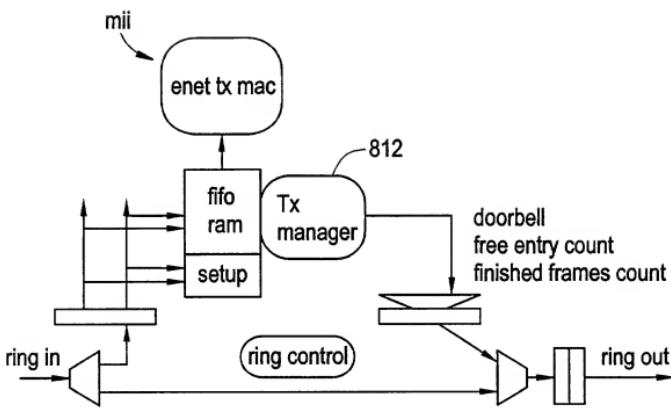




FIG. 70

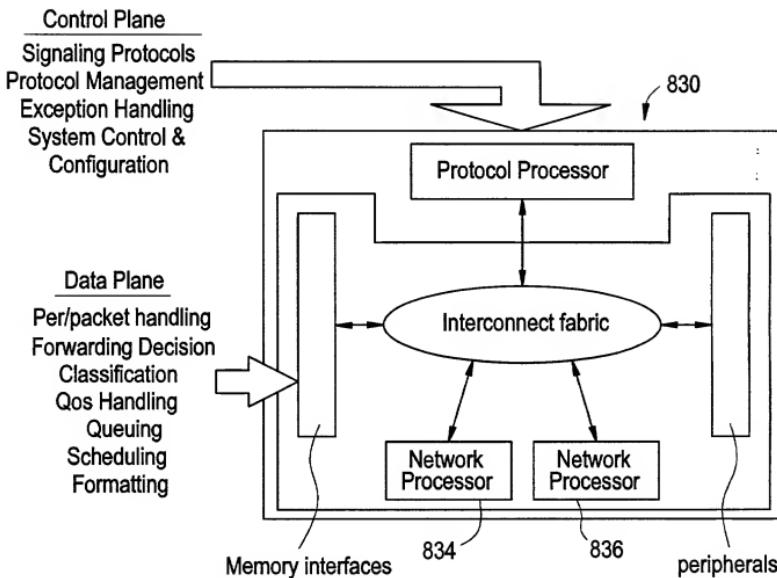


FIG. 71

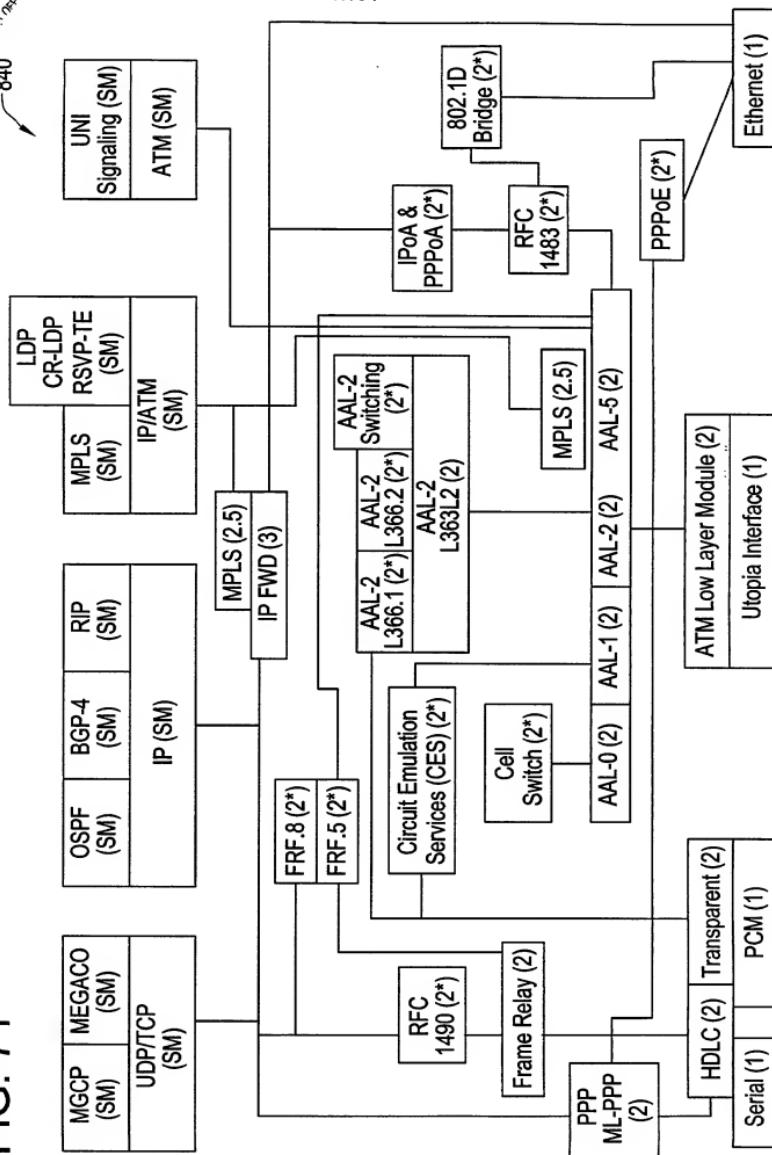




FIG. 72

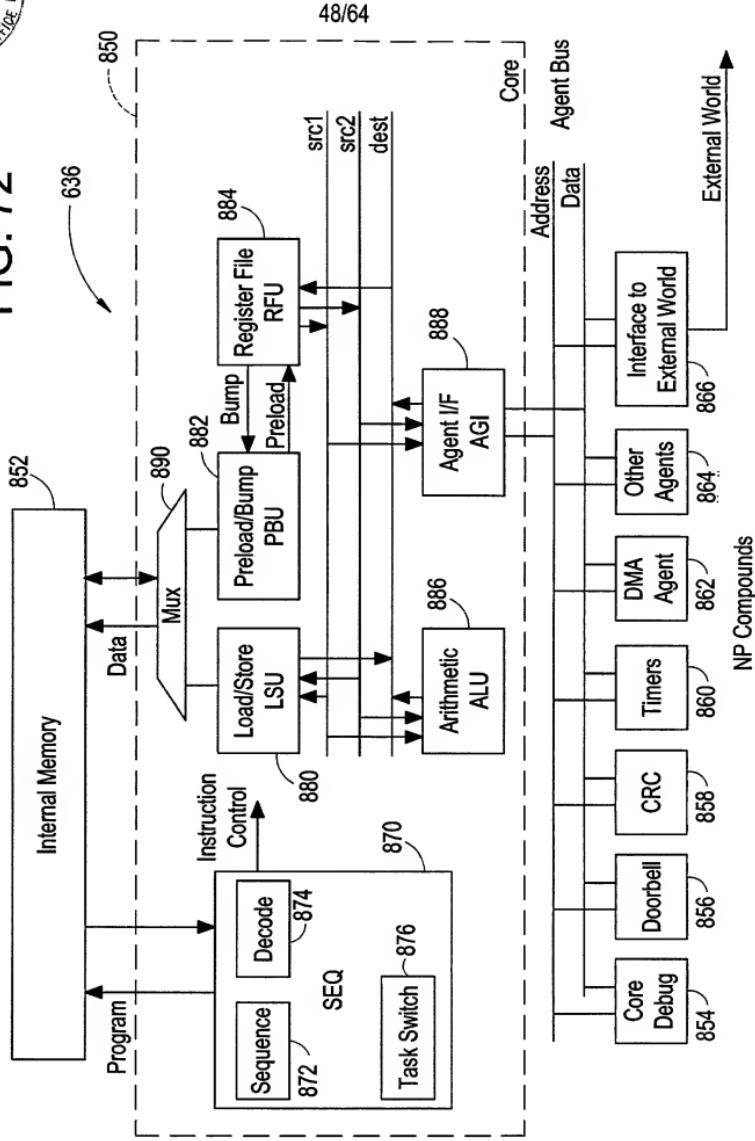


FIG. 73

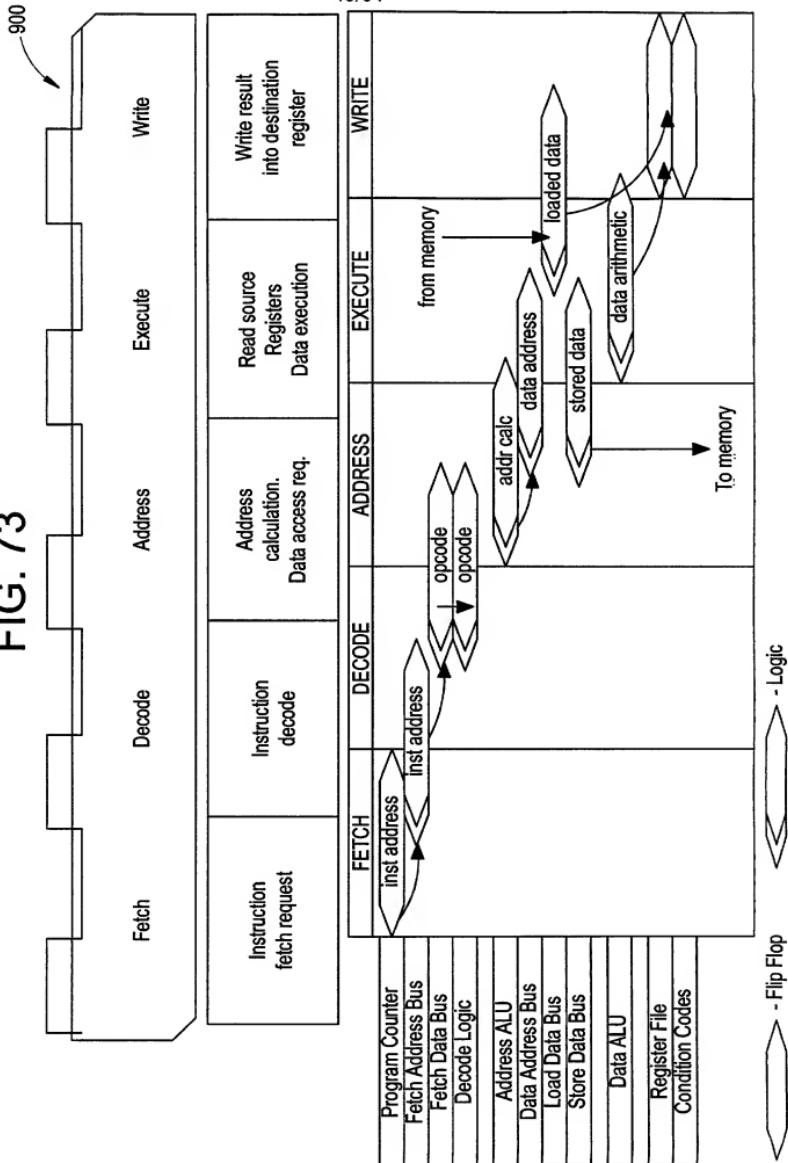


FIG. 74

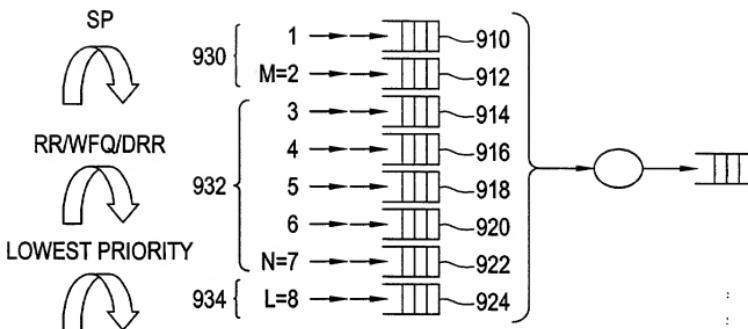
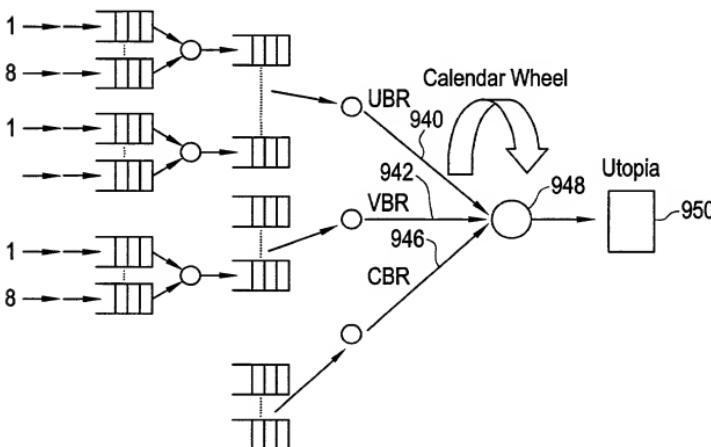


FIG. 75





51/64

FIG. 76

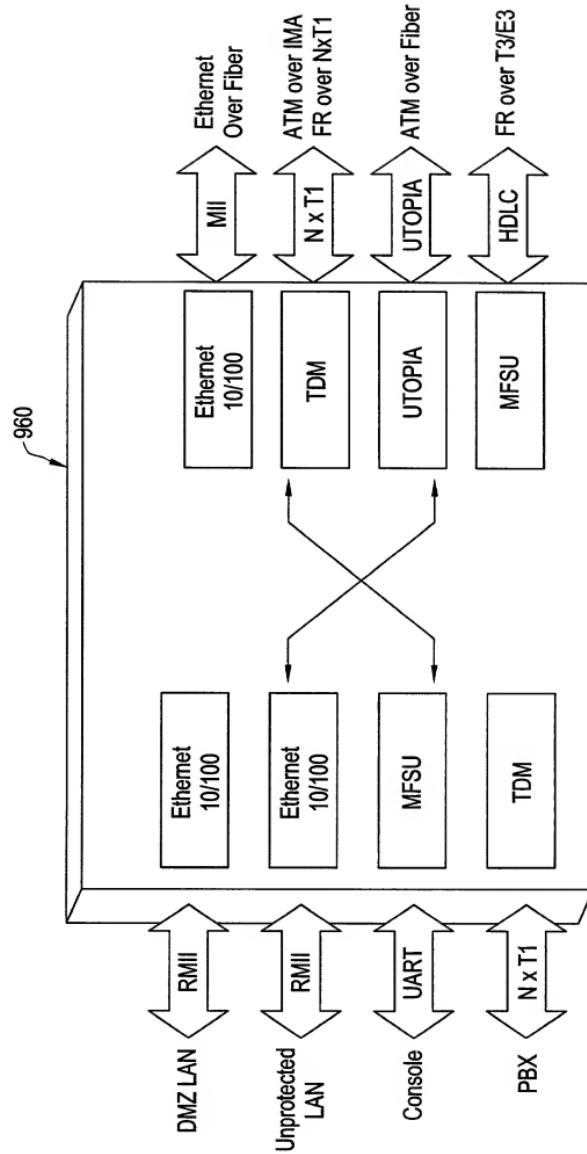


FIG. 77

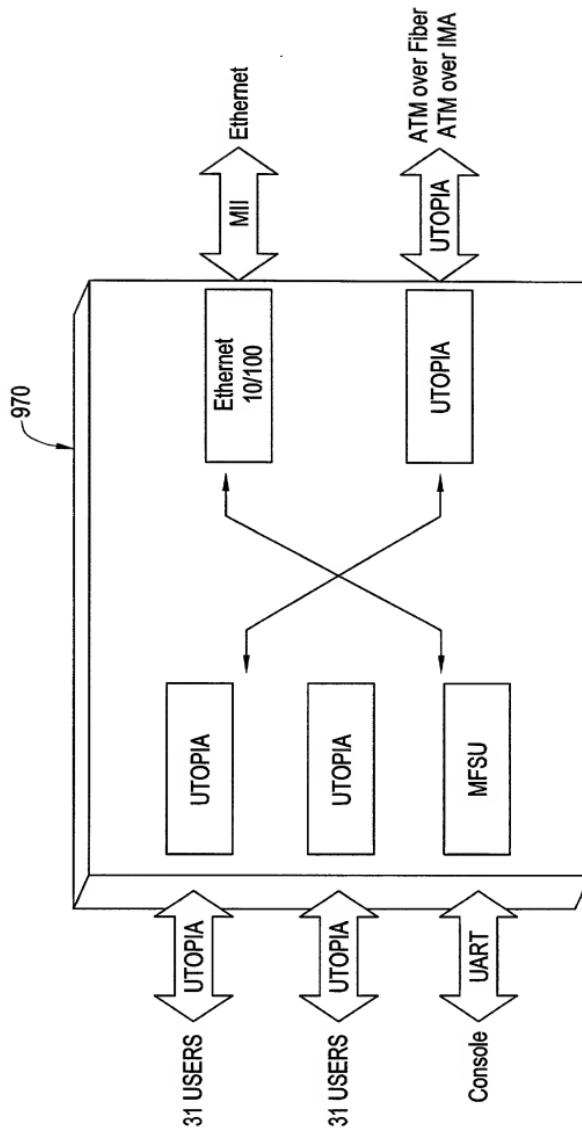


FIG. 78

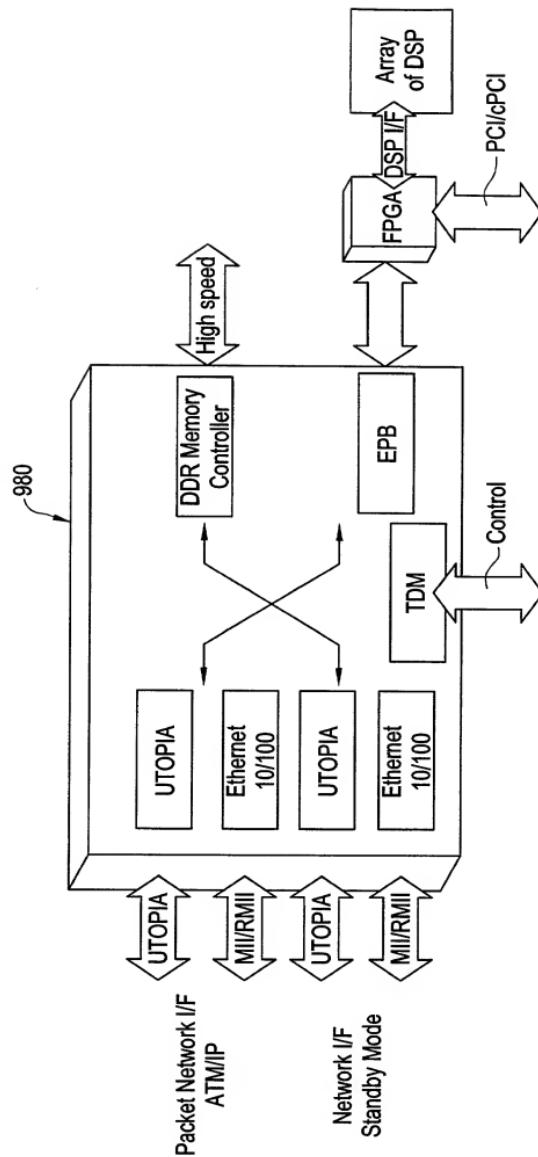


FIG. 79

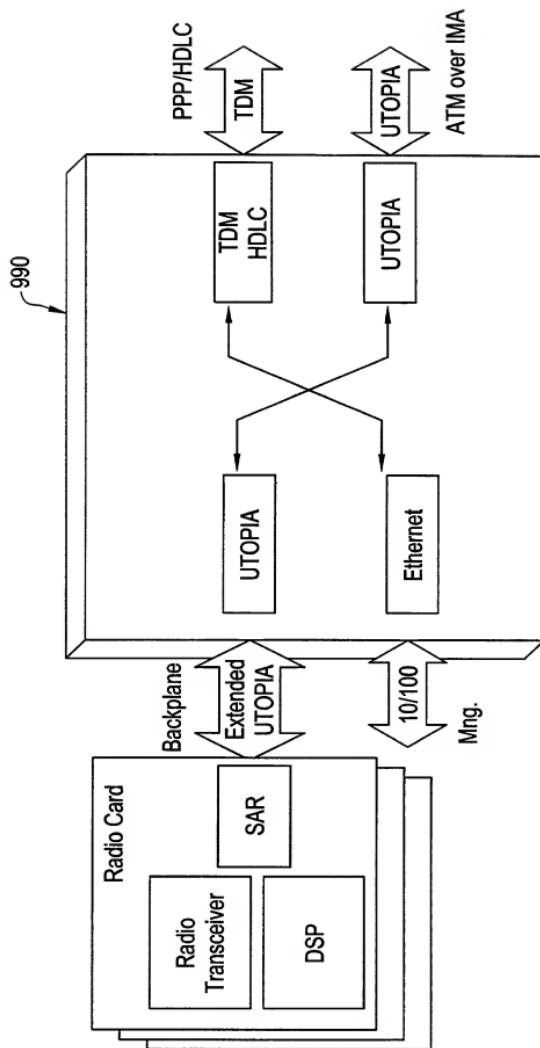


FIG. 80

1000

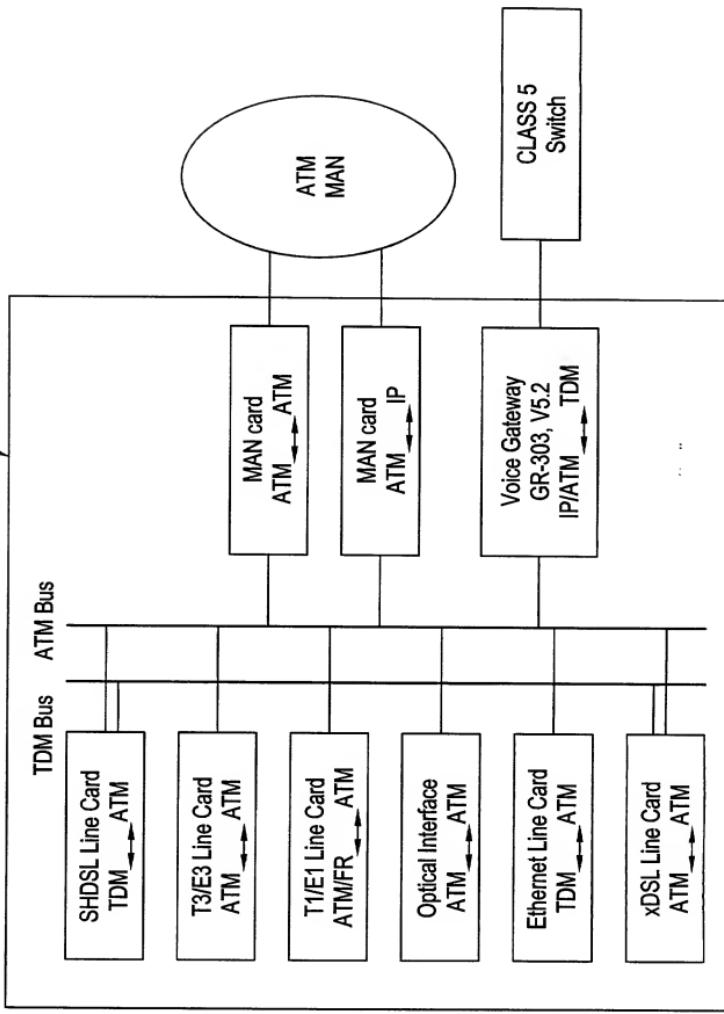


FIG. 81

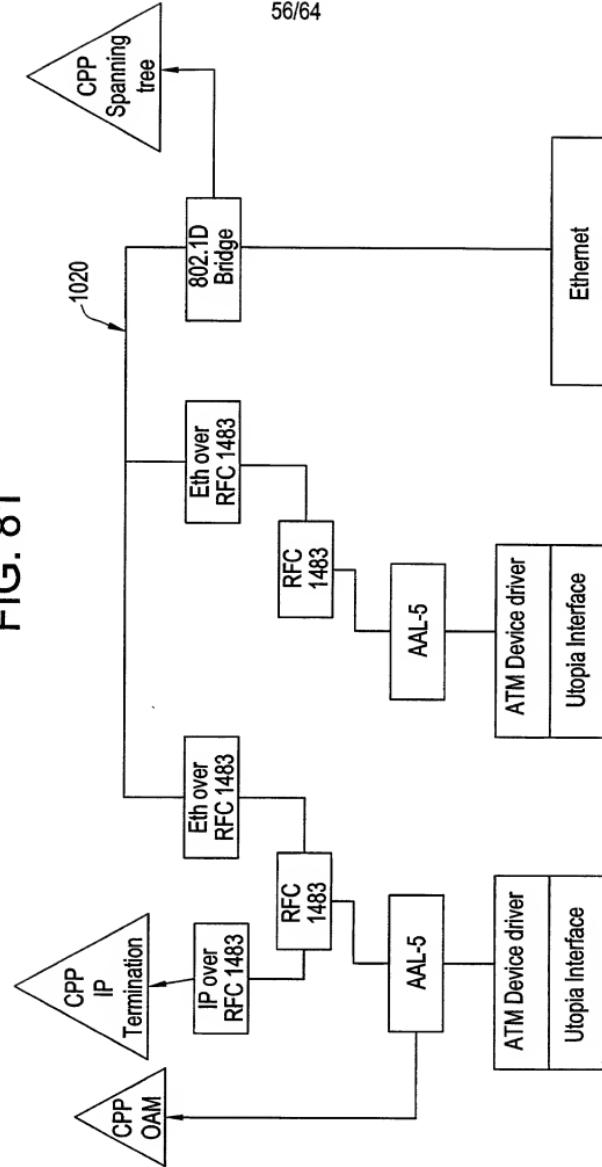


FIG. 82

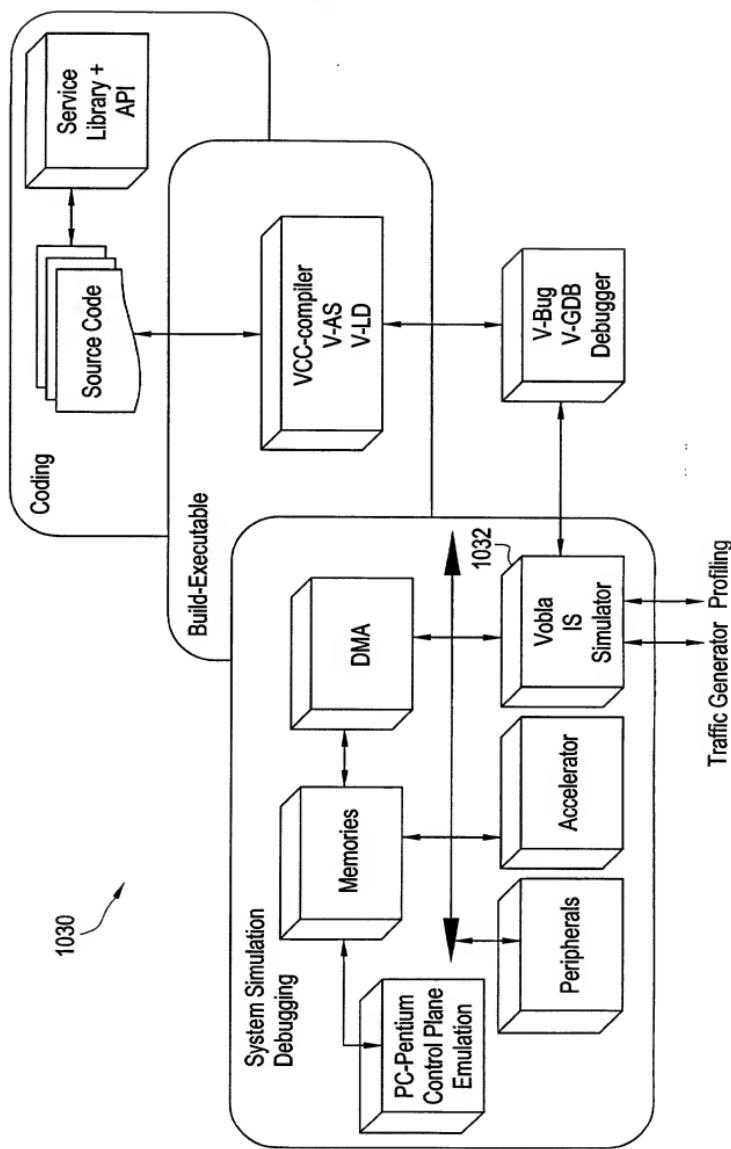


FIG. 83

1040

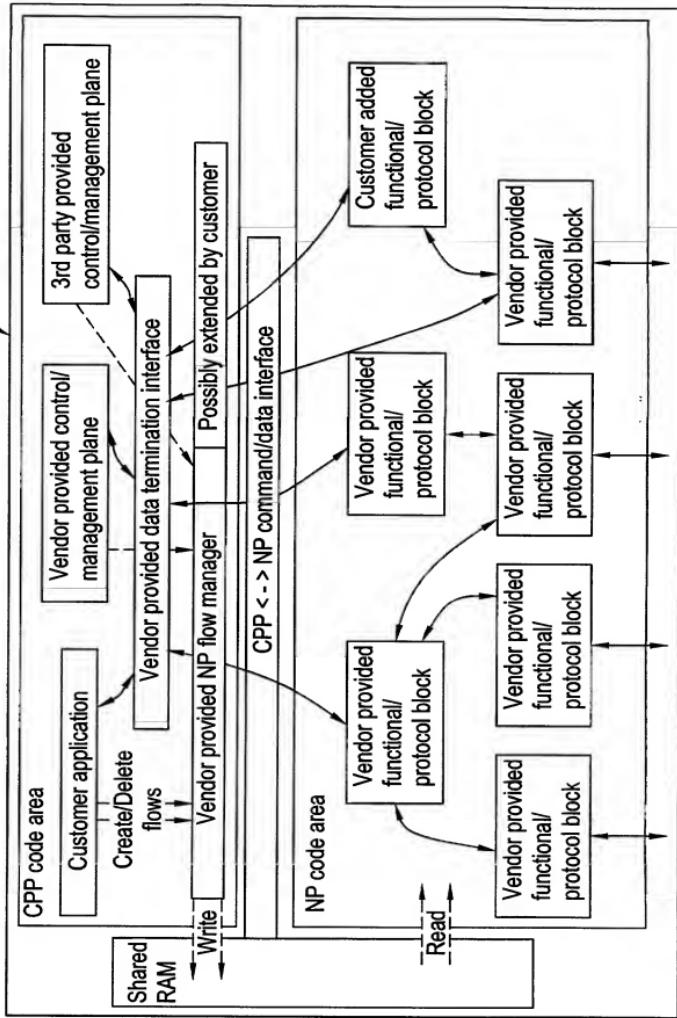


FIG. 84

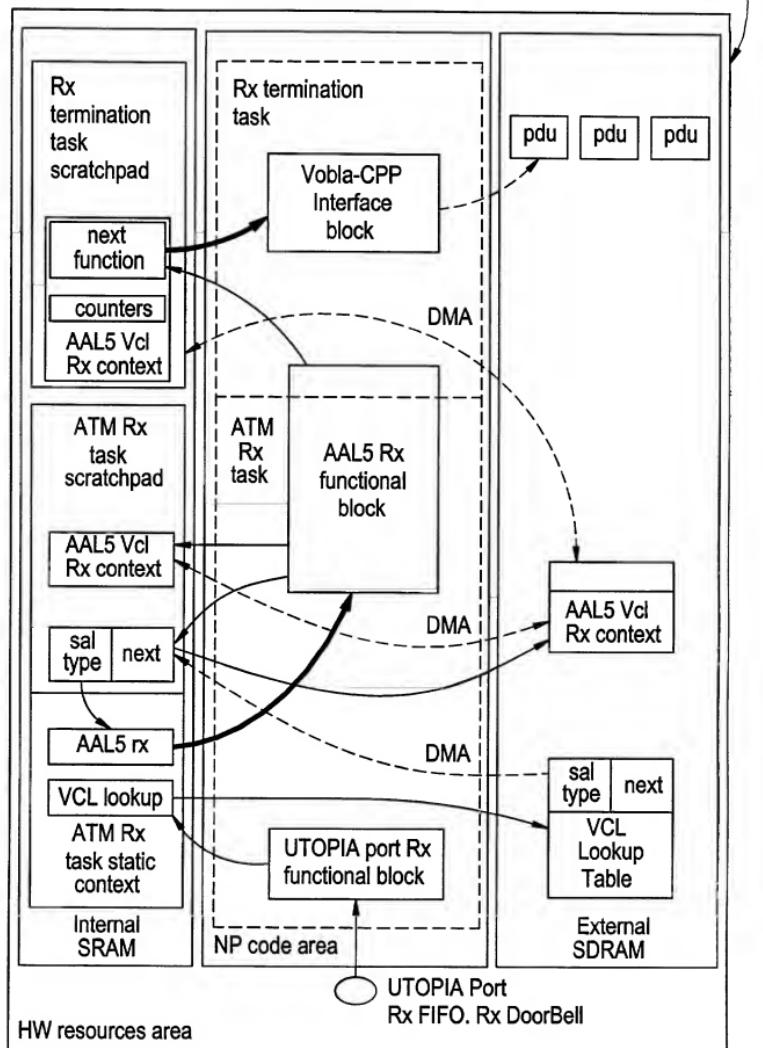


FIG. 85

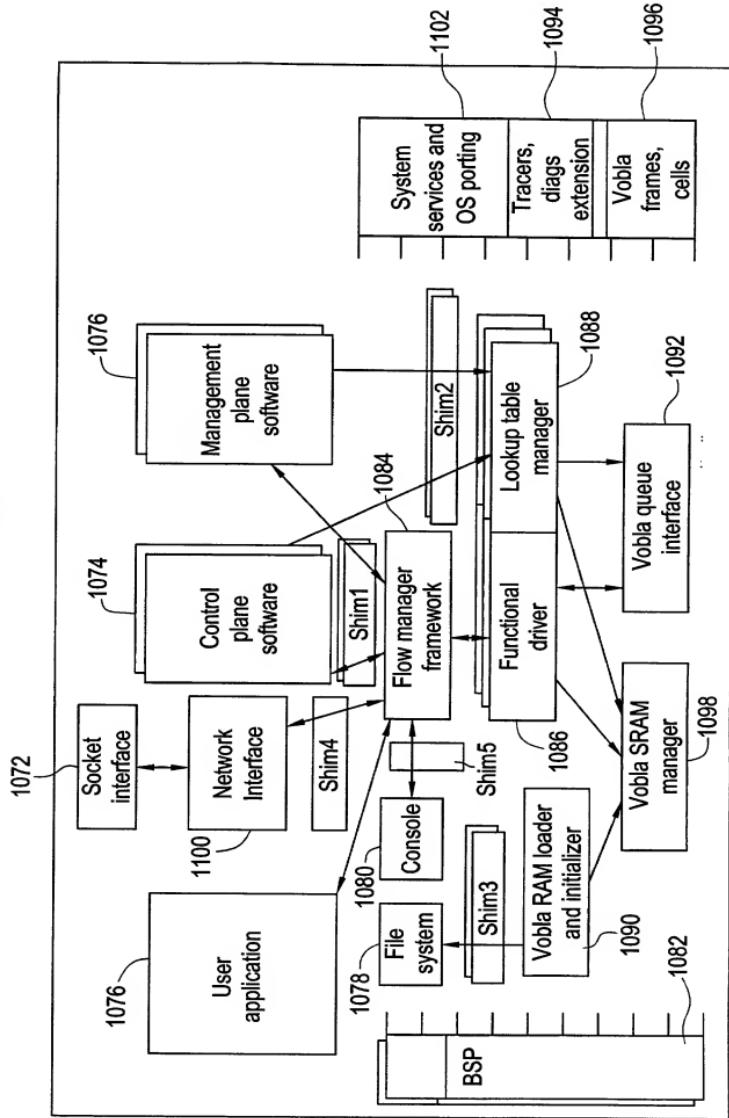
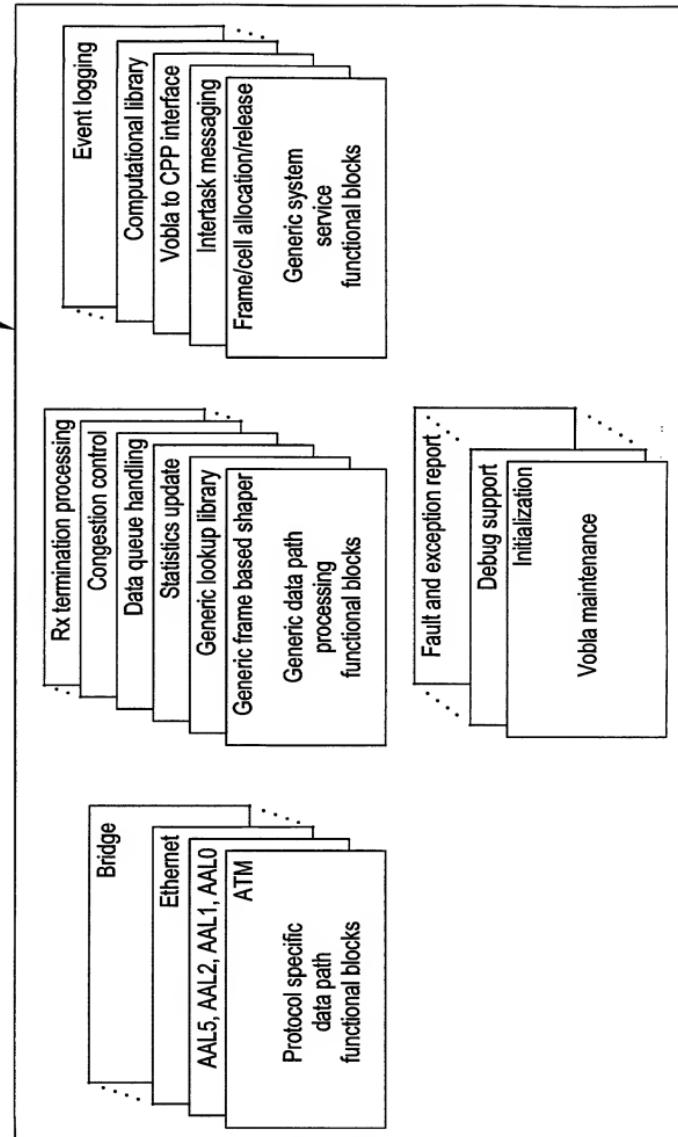




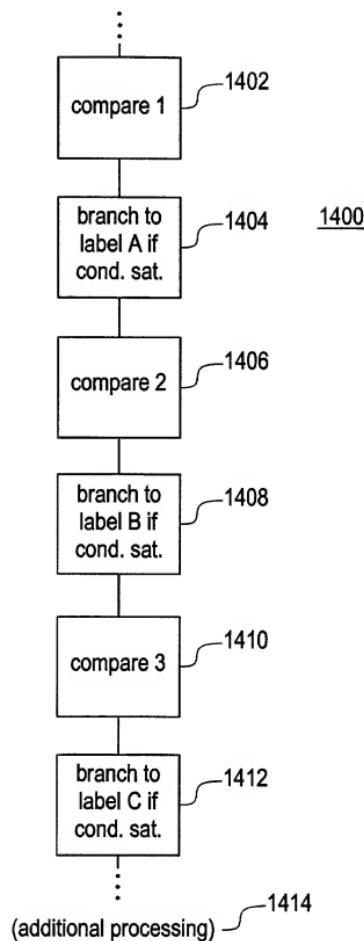
FIG. 86





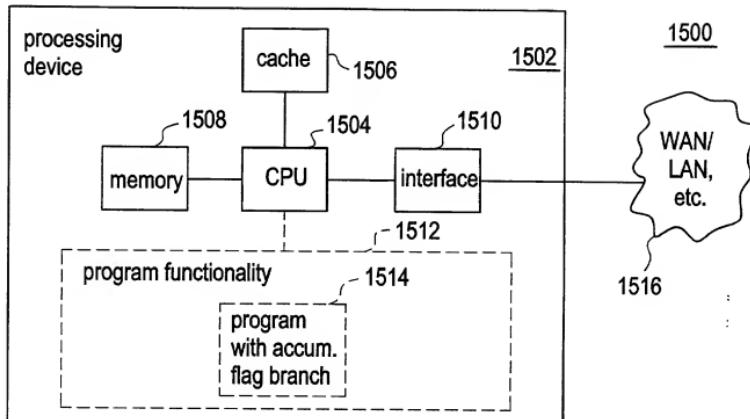
## FIG. 87

## PRIOR ART



20164337.0960

FIG. 88



2042607254930

FIG. 89

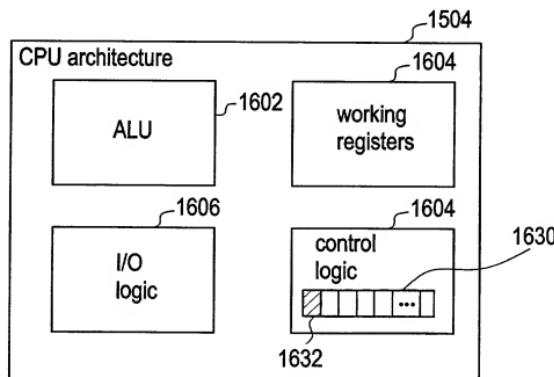




FIG. 90

